Programmes After Market Services
NPM-5 Series Transceivers

CMT Module MA4

Issue 1 11/01

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Glossary of Terms

ACCIF	ACCessory InterFace block of MADLinda
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ARM	Advanced RISC Machines
ASIC	Application Specific Integrated Circuit
AVG	Average
BB	Baseband
BGA	Ball Grid Array package
CCONT	Multifunction power management IC for DCT3
CHAPS	DCT3 Charging control ASIC
CMT	Cellular Mobile Transceiver
COBBA	DCT3 RF-interface and Audio codec IC
COBBA_GJP	Serial control interface version of COBBA
CRFU3	UHF RF IC - used in bl8 RF HW
CSD	Card-specific Data, register in MultiMediaCards
CSP	Chip Scale Package
CTSI	Clocking, Timing, Sleep & Interrupt block of MADLinda
D/A	Digital-to-Analog
DAC	Digital-to-Analog Converter
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCT3	3rd generation Digital Core Technology

DNL	Differential non-linearity
DMA	Direct Memory Access
DL2	RAE-3 Color UI module
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
DTR	Data Terminal Ready
EAD	External Accessory Detect
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FBUS	Full Duplex Serial Bus in NOKIA's phones
FFS	Flash File System
GPIO	General Purpose Input/Output
HAGAR	Direct conversion RF ASIC
HF	Hands Free
HSCSD	High Speed Circuits Switched Data
HW	Hardware
IC	Integrated Circuit
INL	Integral non-linearity
IO	Input/Output
IR	Infrared
IrDA	Infrared Data Association
LCD	Liquid Crystal Display
LEAD	Low power Enhanced Architecture DSP

LNA	Low Noise Amplifier
MAD	MCU+ASIC+DSP chip (**M**CU-**A**SIC-**D**SP)
MAD2	GSM version of MAD
MBUS	1-wire half duplex serial bus in NOKIA's phones
MCU	Micro Controller Unit
MMU	Memory Management Unit
MPU	Micro Processor Unit
NTC	Negative Temperature Coefficient (resistor)
PCI	Phone Control Interface
PCM	Pulse Code Modulation
PLL	Phase Locked Loop
PWB	Printed Wiring Board
PWM	Pulse Width Modulation
R&D	Research and development
RAM	Random Access Memory
RF	Radio Frequency
RFI	RF Interface
ROM	Read Only Memory
RTC	Real Time Clock
SDRAM	Synchronous Dynamic RAM
SIM	Subscriber Identify Module
SW	Software
UI	User Interface
VCTCXO	Voltage Controlled Temperature Compensated Oscillator

VCXO	Voltage Controlled Oscillator

MA4 Module Summary

This section describes the system (CMT) module MA4. The module comprises the RF and baseband functions of the phone.

Baseband

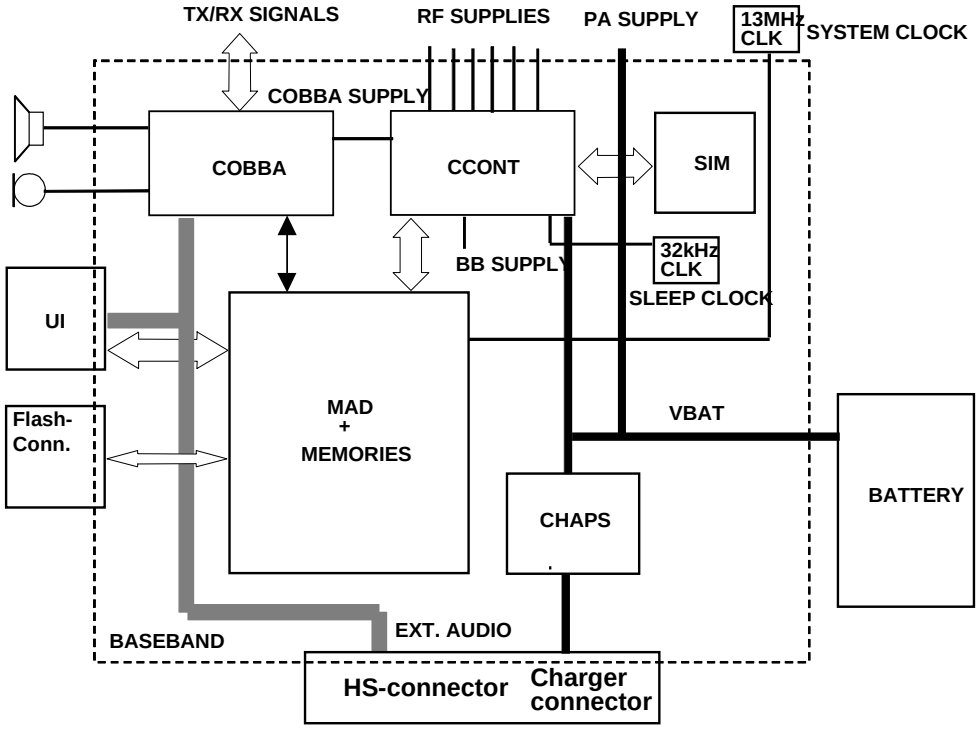


Figure 1: Block Diagram of MA4

Technical Summary

The baseband module includes four ASICs: CHAPS, CCONT, COBBA-GJP and MAD2WD1, which take care of the baseband functions of the engine. All the ASICs are in uBGA package. EEPROM is software emulated in the Flash-memory.

The baseband is designed for direct conversion RF. The baseband is running from a 2.8V power rail (VBB), which is supplied by a power controlling ASIC CCONT.

The CCONT comprises 6 individually controlled regulator outputs for RF-section and two outputs for the baseband. In addition, there is one +5V power supply output (V5V). The CCONT also comprises a SIM interface, which supports both 3V and 5V SIM-cards. A real time clock function is integrated into the CCONT, which utilizes the same 32kHz clock supply as the sleep clock. The battery charging is controlled by a PWM-signal from the CCONT.

The baseband architecture supports a power saving function called "Sleep-mode". In Sleep-mode, the VCTCXO is shut off, which is used as system clock source for both RF and baseband. During the Sleep-mode, the system runs from a 32 kHz crystal.

The phone is waken up by a timer running from this 32 kHz clock supply. The sleeping time is determined by network parameters. The sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock has been switched off.

The MAD2WD1 is a dual voltage circuit using VBB (2.8V Baseband supply) and VCORE (1. 750V. Core Voltage supply for MAD2WD1 ver. C06).

The COBBA ASIC mainly handles the interface between the baseband and the RF section. The COBBA provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface.

The COBBA supplies the analog TXC and AFC signals to RF section according to the MAD2WD1 DSP digital control. Data transmission between the COBBA and the MAD2WD1 is implemented using serial bus for high speed signaling and for PCM coded audio signals.

Digital speech processing is handled by the MAD2WD1 ASIC. The COBBA is a dual voltage circuit, the digital parts are running from the baseband supply VBB (2.8V) and the analog parts are running from the analog supply VCOBBA (2.8V).

The baseband supports both internal and external microphone inputs and speaker outputs. The COBBA selects the source and controls the gain of the input and output signals according to control messages from the MAD.

The MAD generates and encodes the keypad tones, DTMF and other audio tones which then are routed to the COBBA for decoding,

UI-Switch N400 is used as HW-driver for the LEDs, Buzzer and Vibra.

The MAD2WD1 generates the Buzzer and Vibra (internal) alert control signals with separate PWM outputs.

IrDa is not supported.

The phone can be re-flashed in Aftersales using the 4-poled 'Test Flash Connection' pos.: X201 and a Service battery.

EMC shielding is implemented using three metal cans: two for the RF and one for the Baseband. Heat generated by the circuitry is conducted out via the PWB ground planes.

External Signals and Connectors

This section describes the external electrical connection and interface levels on the baseband. The electrical interface specifications are collected into tables that cover a connector or a defined interface.

Test Flash-Connector (X201)

The Test Flash-Connector is used as a flash programming interface for updating (i.e. re-programming) the flash program memory and as an electrical interface for access to the engine by a service tool (e.g. WinTesla). This Interface is used by Aftersales via a 'Service battery'. Refer to Table 1, "Test Flash-Connector," on page 12

The Connector is made via 4 Test Pads which are accessible through the mechanic of the phone when the Battery is removed.

When the flash programming-tool is connected to the phone (via 'Service battery BBS-8'), supply power is provided through the battery contacts and the phone is powered up with an IBI-pulse given to the BTEMP line**.**

***Note**: ESD protection is applied to all pads of X201.*

Table 1: Test Flash-Connector

Pin	Name	Parameter	Min.	Typ	Max	Unit	Remark
1	FBUS_TX	Data ack. to the Prommer	0 2.24	logic low logic high	0.62 2.85	V	Transmit Data from MAD2WD1 (AccTxData) to Prommer (@ VBB=2,85V)
2	FBUS_RX	Serial data from the Prom-mer	0 1,68	logic low logic high	0.84 2.85	V	Receive Data from Prommer to MAD2WD1 (AccRxData) (@ VBB=2,85V)
3	GND	GND	0		0	V	Ground
4	MBUS	Serial clock from the Prom-mer	0 1,68	logic low logic high	0.84 2.85	V	Prommer detection and Serial Clock for synch. Comm. to MAD2WD1 (MBUS) (@ VBB=2,85V)

Battery Connector (X203)

The electrical specifications for the battery connector are shown in Table 2, "Battery Connector," on page 13. The BSI contact on the battery connector is used to detect when the battery is removed. This is to be able to shut down the operations of the SIM card before the power is lost if the battery is removed with power on.

The BSI contact disconnects earlier than the supply power contacts to give enough time for the SIM shut down

Table 2: Battery Connector

Pin	Name	Min.	Typ	Max	Unit	Notes
1	VBATT	3.1	3.6	5.2	V	Battery voltage
2	BSI	0		2.85	V	Battery size indication Phone has 150kohm pull up resistor. SIM Card removal detection (Threshold is 2.4V@VBB=2.8V)
		2,2		51	Kohm	"Nickel Battery" Size indication resistor
			22		Kohm	"Service Battery" indication resistor
		56		130	Kohm	"4.2v Lithium Battery" Size indication resistor
3	BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+-5%) pullup resistor, Battery package has a NTC pulldown resistor.
		2.1 5	10	3 20	V ms	Phone power up by battery (input) Power up pulse width (IBI)
4	GND	0		0	V	Battery Ground is connected directly to GND.

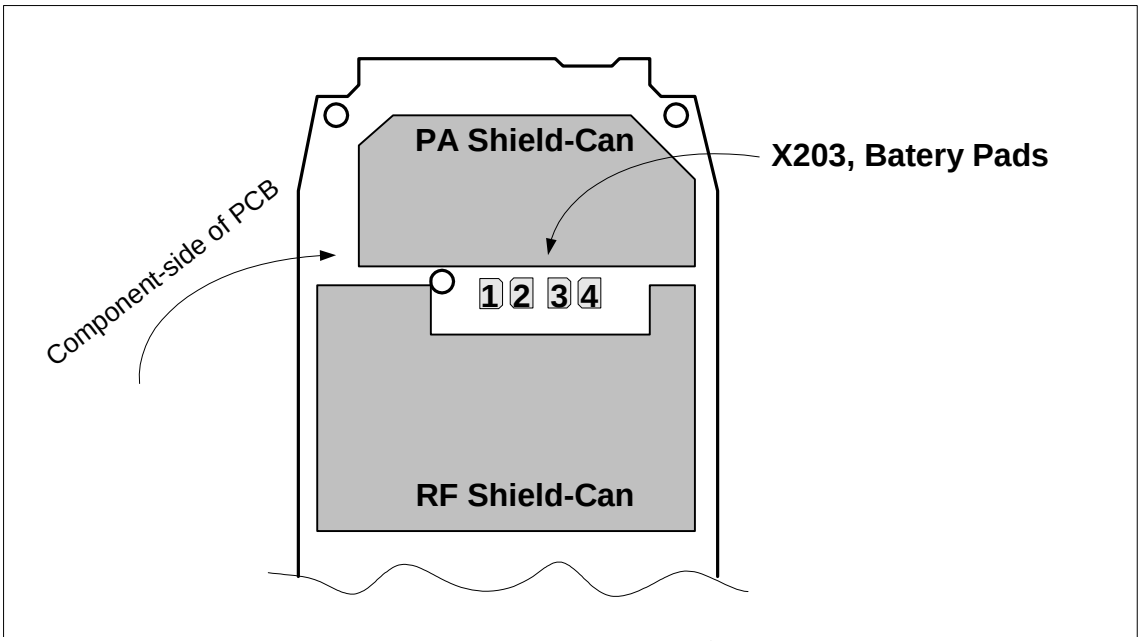


Figure 2: X203 Battery Pads

SIM card connector (X400)

The SIM I/F does not support other voltages than 3V and 5V. Refer to Table 3, "SIM Connector," on page 14

The SIM card connector is located outside the BB-shield can close to the System Connector.

Table 3: SIM Connector

Pin	Name	Parameter	Min.	Typ	Max	Unit	Notes
1	SIMCLK	Frequency Trise/Tfall		3.25	 25	MHz ns	SIM clock
2	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	"1" "1"	VSIM VSIM	V	SIM reset
3	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
4	GND	GND	0		0	V	Ground
5	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	"1" "0" "1" "0"	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us

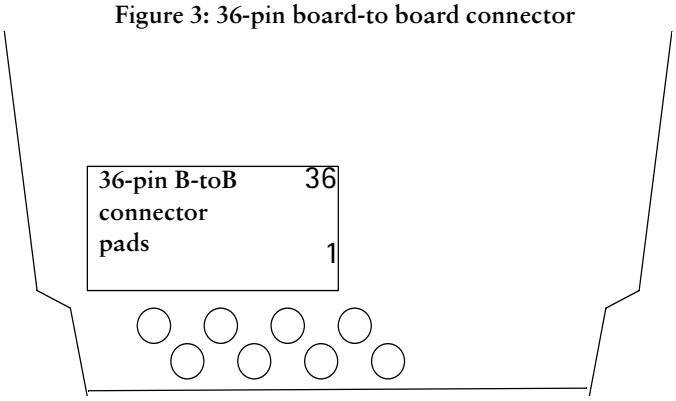
VSIM supply voltages are specified to meet type approval requirements regardless the tolerances in components.

Internal Signals and connections

36-pin board to board connector

CMT module has landing pads for 36-pin spring connector. See "Board -to board connector pins" on page 15. Below picture shows its placement on bottom layer of PWB. View is taken from bottom side. Below this 36-pins spring connector pads are production flash connectors round pads.

Figure 3: 36-pin board-to board connector



Pin numbering goes from pin 1 to left. Pin 36 is just above pin 1.

Table 4: Board -to board connector pins

Pin	Name	Min.	Typ	Max	Unit	Notes
1	PURX	0		VBB	V	Power up reset from radio module, active low
2	CHRGR+	0	8.4	16.9	V	Raw charging voltage from charge connector on ui board to charge IC on phone PWB
3	LCDRSTX	0 0.7xVBB	low high	0.3xVBB VBB	V	LCD Reset output Active low
4	GND	0	0	0	V	
5	GENSIO(0)	0 0.7xVBB	low high	0.3xVBB VBB 4	V MHz	LCD Serial clock output
6	VBB	2.7	2.8	2.85	V	Regulated supply voltage from phone, only for I/O voltage reference and phone power on indication
7	GENSIO(1)	0 0.7xVBB	low high	0.3xVBB VBB	V	LCD Serial data output
8	VB	3.1	3.6	5.2	V	Supply voltage from battery
9	LCDENX	0 0.7xVBB	low high	0.3xVBB VBB	V	LCD Chip select output Active low
10	ROW5	0 0.7xVBB	low high	0.3xVBB VBB	V	LCD Control input
11	VB	3.1	3.6	5.2	V	Supply voltage from battery
12	ROW4	0 0.7xVBB	Low high	0.3xVBB VBB	V	General purpose input or output pin to radio module.
13	ROW3	0 0.7xVBB	Low high	0.3xVBB VBB	V	General purpose output pin to radio module.
14	GND	0	0	0	V	
15	ROW2	0 0.7xVBB	Low high	0.3xVBB VBB	V	General purpose input pin to radio module
16	KBDLEDS	0		VBB	V	Keyboard led drive current sink (60mA) for 4 LEDS
17	LCDLEDS	0		VBB	V	Display led drive current sink (60mA) for 4 LEDS
18	VBB	2.7	2.8	2.85	V	Regulated supply voltage from phone, only for I/O voltage reference and phone power on indication
19	CHRGR+	0	8.4	16.9	V	Raw charging voltage from charge connector on ui board to charge IC on phone PWB
20	VB	3.1	3.6	5.2	V	Supply voltage from battery

Pin	Name	Min.	Typ	Max	Unit	Notes
21	FBUSRX	0 1.68	Low high	0.84 2.85	V	Serial interface between UI and radio module. Output from UI module
22	MBUS	0 1,68	low high	0.84 2.85	V	Prommer detection. (@ VBB=2,85V)
23	FBUSTX	0 2.24	Low high	0.62 2.85	V	Serial interface between UI and radio module. Input to UI module
24	GND	0	0	0	V	
25	XMICN					External Microphone - HS(5)
26	XMICP					External Microphone + HS(7)
27	GND	0	0	0	V	
28	XEARP					External Earpiece + HS(8)
29	XEARN					External Earpiece - HS(6)
30	GND	0	0	0	V	
31	EAR-					Internal Earpiece - HS(2)
32	EAR+					Internal Earpiece + HS(1)
33	GND	0	0	0	V	
34	MIC-					Internal Microphone - HS(3)
35	MIC+					Internal Microphone + HS(4)
36	GND	0	0	0	V	

Power Distribution

In normal operation, the baseband is powered from the phone's battery.

An external charger can be used for recharging the battery and supplying power to the phone.

The baseband contains parts that control power distribution to whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to the CCONT and UI (buzzer and LEDs for display/ keyboard). Figure 4, "Baseband Power Distribution," on page 17 shows a block diagram of the power distribution.

The power management circuit CHAPS provides protection against over-voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.

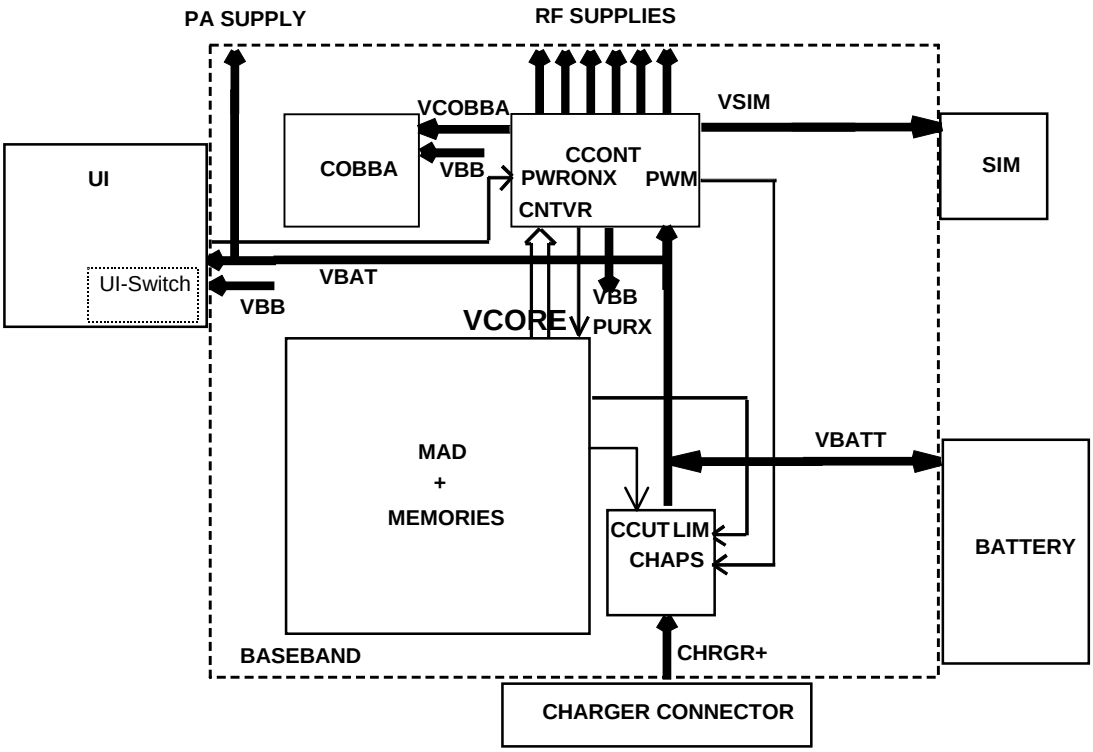


Figure 4: Baseband Power Distribution

Battery Charging

The phone supports both 2-wire and 3-wire Nokia chargers, but when using 3-wire chargers, then the phone connects the 3rd. wire (charger control input) to Ground.

At the DC connector input (CHRGR+) the absolute maximum input voltage is 30V. At the phone end there is no difference between a plug-in charger and a desktop charger because the DC-jack pins and bottom connector charging pads are connected internally in the System connector. The control-line of three terminal chargers is connected to GND on the PCB. Charger ground is also connected directly to GND on the PCB.

The CCUT MAD-signal controls the CTIM-pin. When CTIM is shorted (CCUT = '1'), the CHAPS stops charging. During detection of accessories the charging is stopped to prevent, that 'high' charge current will disturb the sensible A/D-measurement.

Start-up Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level reaches 3.0V (+/- 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software.

If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken

control over the charging, the startup current is switched off.

The startup current is switched on again when the battery voltage has dropped 100mV (nominal).

Table 5: Startup Characteristics

Parameter	Symbol	Min.	Typ	Max	Unit
VOUT Start- up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start- up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start-up regulator output current VOUT = 0V. Vstart	Istart	130	165	200	mA

Battery over-voltage protection

The CHAPS includes an over-voltage protection circuit (input pin VBAT), which purpose is to protect the phone from damage caused by too high Battery voltage.

The MAD selects the different cutoff voltages (VLIM1 or VLIM2) for the two different battery types (Li or Ni) via CHAPS-input pin LIM according to the table below

Table 6: VLIM Characteristics

Parameter	Symbol	LIM input	Min.	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM1	LOW	4.4	4.6	4.8	V
Output voltage cutoff limit (Ni-battery)	VLIM2	High	4.8	5.0	5.2	V

The internal power switch is immediately turned OFF, if the voltage at CHAPS-input pin VBAT rises above the selected limit VLIM.

When the internal power switch has turned OFF because of an overvoltage detection, it stays OFF until the Charger-voltage drops below Vpor (CHAPS Power On Reset Threshold) ($Vpor_{min.}$ = 2.8V, $Vpor_{max.}$= 3.12V). It is necessary to reconnect the charger to reset the VLIM protection.

The VBAT input of the CHAPS is connected through a 120R resistor to the battery voltage at a sense point close to the battery (see Figure 7, “Standard Battery, BTEMP Connection,” on page 21). A 1uF Capacitor is placed at the VBAT pin close to the CHAPS and it acts with the 120R resistor as a filter to reduce influences of fast overvoltage transients caused by the Charger Switch or when connecting the charger.

A voltage divider (120R + 3K3) on the VBAT input of the CHAPS is only active during charging which is controlled by a transistor activated by the MAD signal CHAR_CTRL. The voltage divider reduces the Sense voltage by approx. 175mV +/-25mV, which gives new values for VLIM as shown below:

$VLIM2_{min}$ = 4.95V
$VLIM2_{max}$ = 5.4V

Battery removal during charging

Output over-voltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM, CHAPS turns switch OFF until the charger input has sunken below Vpor (Vpor $_{min.}$ = 2.8V, Vpor $_{max}$.= 3.12V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed.

PWM

When a charger is connected, the PWM input turns the power switch ON and OFF.

The PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current - CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. Soft switching is used to prevent the switching transients inducing noise in audio circuitry of the phone.

Battery identification (BSI)

Different battery types are identified by a pull-down resistor inside the battery pack. In the baseband area of the transceiver, the BSI line has a 150k pull-up to VBB. The MCU can identify the battery by reading the BSI line DC-voltage level with a CCONT (N201) A/D-converter.

Table 7: Battery Identification

Name	Min.	Typ	Max	Unit	Notes
BSI	0		2,85 (VBB)	V	**B**attery **S**ize **I**ndication pull-up to VBB = 150k ± 5% SIM Card removal detection Threshold = 2.4V@VBB=2.8V
RS	-1%	3,3	+1%	Kohm	Indication resistor for BMC-2 battery (640mAh, NiMH)
Rs	-1%	5,6	+1%	Kohm	Indication resistor for BMC-3 battery (900mAh, NiMH)
Rs	-1%	75	+1%	Kohm	Indication resistor for BLC-2 battery (900mAh, 4.2v Lilon)
Rs	-1%	22	+1%	Kohm	Indication resistor for service battery

Note: *No support of 4.1v lithium*

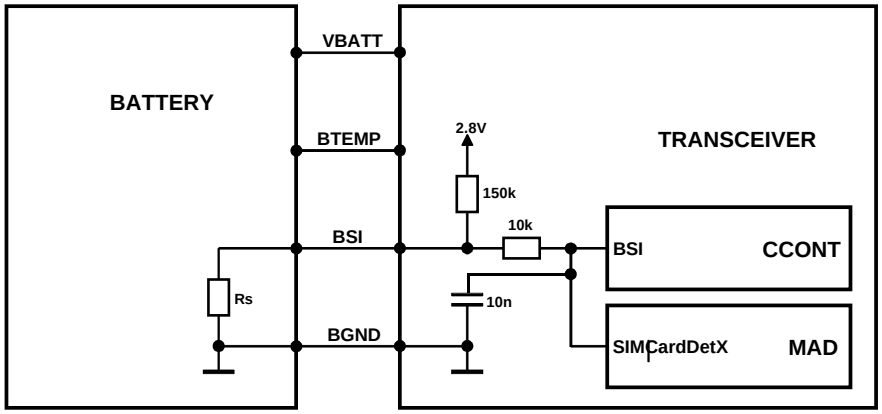


Figure 5: BSI Connections - All Batteries

The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2. SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery contact disconnects before the other contacts so that there is a delay between battery removal detection and supply power off.

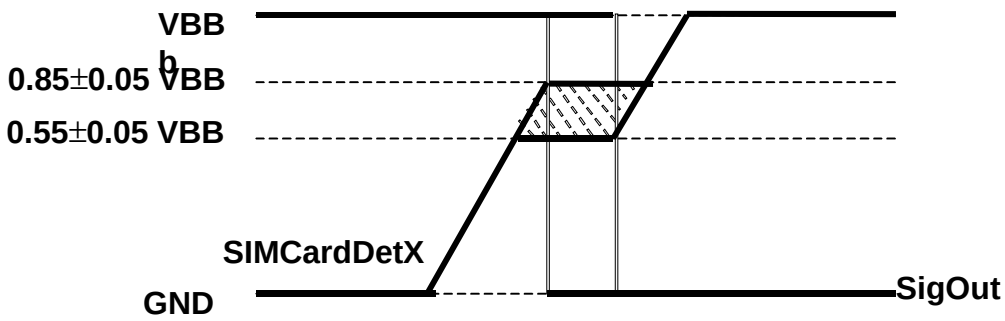


Figure 6: SIMCardDetX Detection Levels

Battery temperature (BTEMP)

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pull-up to VREF. The MCU calculates the battery temperature by reading the BTEMP line DC-voltage level with a CCONT (N201) A/D-converter.

Table 8: Battery Temperature

Name	Min.	Typ	Max	Unit	Notes
BTEMP	0		VREF	V	Battery temperature indication 100k pull-up resistor to VREF in phone Battery package has NTC pull down resistor.
	2.1 5	10	3 20	V ms	IBI-pulse, Phone power up by battery (input) Power up pulse width
	-5				100k pull-up resistor tolerance

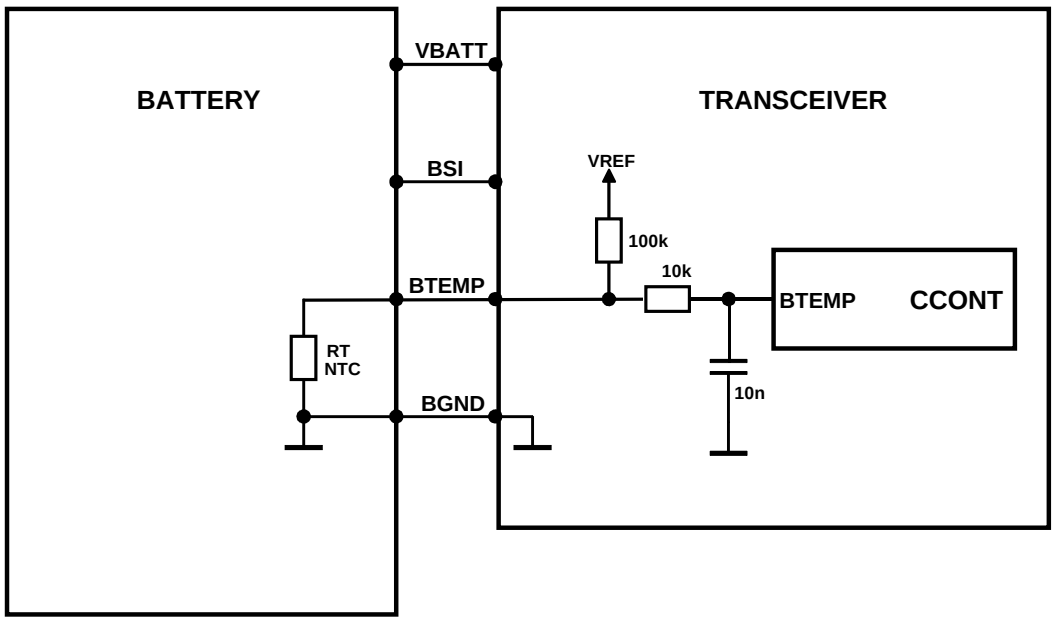


Figure 7: Standard Battery, BTEMP Connection

Supply voltage regulators

The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD2WD1 and memories, COBBA digital parts and the LCD driver in the UI section.

There is a separate regulator for the SIM card. The SIMPwr line from MAD2WD1 to CCONT controls the regulator, selectable between 3V and 5V. The COBBA analog parts

are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF.

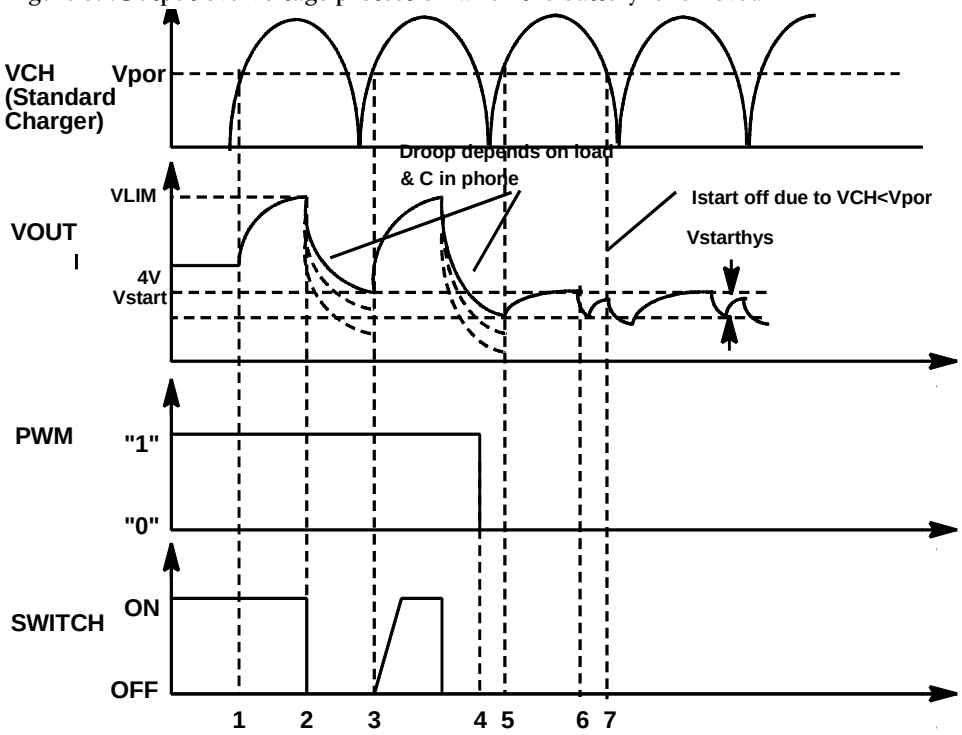
Table 9: Regulator Activity - Different Operating Modes

Operating mode	Vref	RF REG	VCOBBA	VCORE	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On	On/Off
Reset	On	Off VR1 On VR6 On	On	On	On	Off	Pull down
Sleep	On	On/Off	Off	Off	On	On	On/Off

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators are controlled by SW via the serial Bus GENSIO(1:0) from the MAD2WD1.

CCONT generates also a 1.5 V reference voltage VREF to COBBA. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

Figure 8: .Output overvoltage protection when the battery is removed



1. **Battery removed, (standard) charger connected, VOUT rises (follows charger**
2. **VOUT exceeds limit VLIM(X), switch is turned immediately**
3. **VOUT falls (because no battery) , also VCH<Vpor (standard chargers full-output). When VCH > Vpor and VOUT < VLIM(X) -> switch turned on again (also is still HIGH) and VOUT again exceeds**
4. **Software sets PWM = LOW -> CHAPS does not enter PWM**
5. **PWM low -> Startup mode, startup current flows until Vstart limit**
6. **VOUT exceeds limit Vstart, Istart is**
7. **VCH falls below**

Switched mode power supply VSIM

There is a switched mode supply for SIM-interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

Table 10: Electrical Characteristics of VSIM and V5V

Characteristics	Condition	Min.	Typ	Max	Unit
Output voltage VSIM	Over temperature Over current	2.8 4.8	3.0 5.0	3.2 5.2	V
Output voltage V5V	Over temp & current	4.8	5.0	5.2	V
Output voltage V5V_2	Over temperature	5.0		6.0	V
Output current VSIM	Continuous DC			30	mA
Output current V5V	Continuous DC			30	mA
current consumption VSIM	on sleep		200 100	330 150	uA uA

Note: *VSIM and V5V together can supply a total of 30mA.*

SMR / VSIM-functions is shown below.

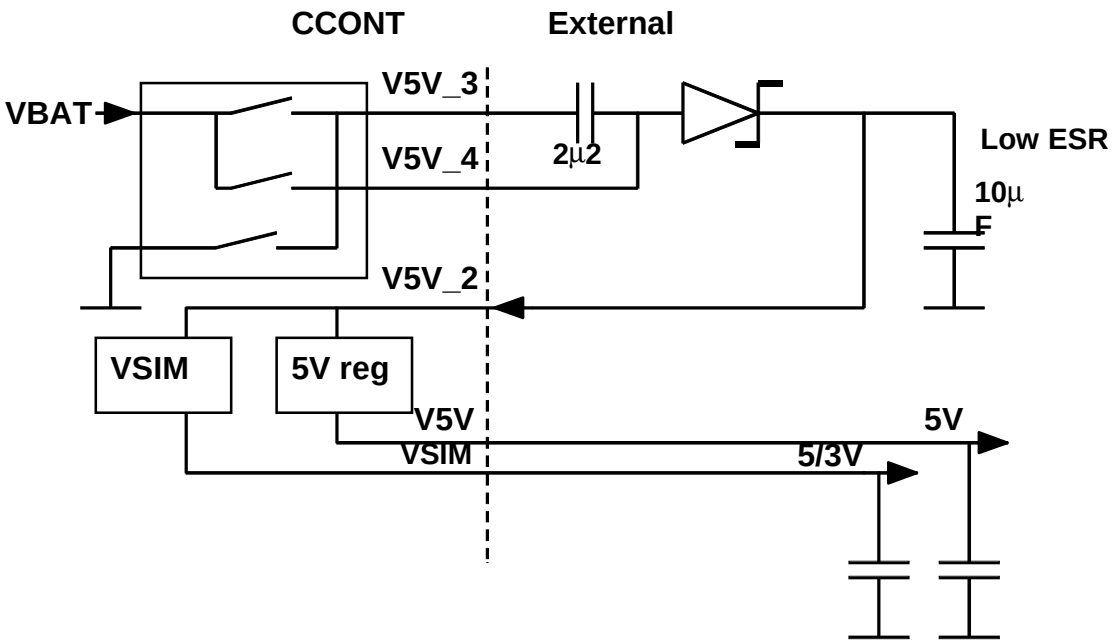


Figure 9: SMR Power Functions

Power Up and Power Down

When the PURX reset is released, the MAD2WD1 releases the System-reset signals (Ext-SysResetX and the internal MCUResetX) and starts the boot program execution.

In normal operation, the program execution continues from the flash program memory. However, If the MBUS line is pulled low during the power up, then the boot-ROM starts a flash programming sequence and waits for the prommer response through FBUS_RX line.

The baseband is powered up by:

1. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

2. Pressing the power key, that generates a PWRONX signal from the power key to the CCONT, this starts the power up procedure.

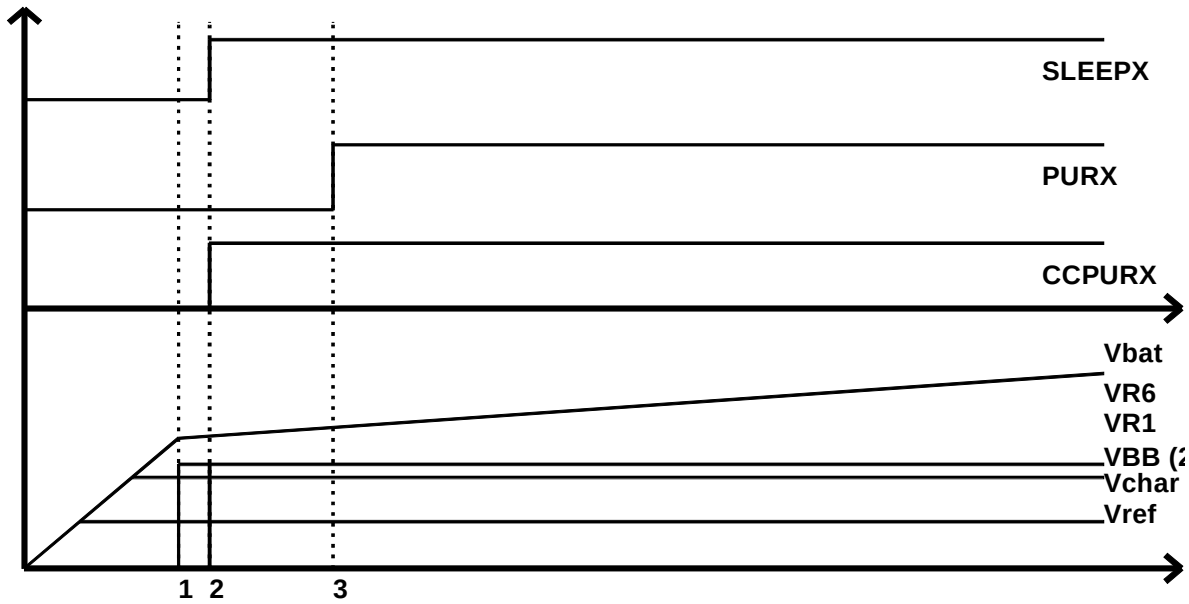
3. A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PURX line to give a power on signal to the CCONT just like the power key.

4. IBI-pulse. When a short (10ms) voltage pulse is applied to the BTEMP pin, the CCONT wakes up and starts the power on procedure. This is used by the Service tools.

Power up with a charger

When the charger is connected, CCONT will switch on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD2WD1 in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay, MAD2WD1 reset is released, and VCXO -control (SLEEPX) is given to MAD. The next diagram (Figure 10, "Power Up with Charger," on page 25) explains the power on procedure with charger (the picture assumes empty battery, but the situation would be the same with full battery)

:



1: Battery voltage over 3.0==>Digital voltages to CCONT
2: CCONT digital reset released. VCXO turned on
3: 62ms delay before PURX

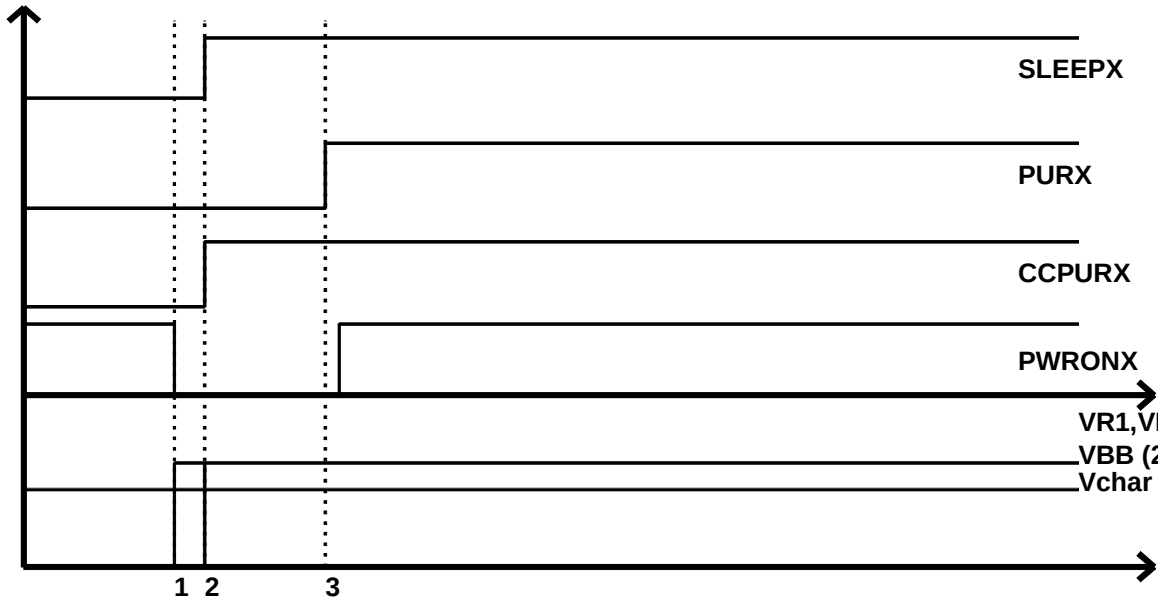
Figure 10: Power Up with Charger

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard power-up procedure and the power-up is delayed.

Power up with power switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO, as was the case with the charger driven power up. If PWRONX is low when the 62 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 62 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts). Refer to Figure 11, "Power-up with switch," on page 26.

Figure 11: Power-up with switch



1: Power switch pressed ==> Digital voltages on in CCONT.
2: CCONT digital reset released. VCXO turned on.
3: ≈ 62 ms delay.

Power up by RTC

When the user selects the Alarm, and the phone is powered off, the RTC (internal in CCONT) powers up the phone at the alarm set time (internal CCONT signal RTCPwr set to logical 1).

Power up by IBI

IBI can power CCONT up by giving a short pulse (10ms) through the BTEMP line. After power-up BTEMP will act as any other input channel for ADC.

Power Down

The baseband is powered down:

- Pressing the power key (that the MAD monitors).
- The battery voltage has dropped below the operation limit, either by not charging it or by removing the battery.
- Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.
- Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the user turns the alarm off. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT as the power key does.

The MAD controls the power down. When the power key has been pressed long enough, or the battery voltage is dropped below the limit, the MCU initiates a power down proce-

dure and disconnects the SIM power. Then the MCU outputs a system-reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself.

After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the CCONT powers the phone down.

Modes of Operation

Acting Dead

If the phone is off or switched off when the charger is connected, the phone is powered on but enters a state called"acting dead". To the user, the phone acts as if it was switched off. A battery-charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

Sleep Mode

In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. The MAD2WD1activates the Sleep mode after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low.

In this state, only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD2WD1 or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD2WD1 starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high.

After VCXO settling-time other regulators and clocks are enabled for active mode. If the battery pack is disconnected during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging is allowed in any operating mode. For Ni-MH batteries the max. charging temperature is +48°C. Above this temperature the charging algorithm is changed to 'hot-charge' which means that only the amount of current that is taken out from the battery is charged at the same time to the battery.

The battery type/size is indicated by a resistor inside the battery pack. The resistor value

corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

Energy Management software running in the MAD controls the CCONT which measures the battery voltage, temperature, size and current.

The Energy Management controls the charging current delivered from the charger to the battery. The CCONT generates a PWM input signal which controls the charging.

The CHAPS switch tuns off when the battery voltage has reached 5.2V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Watchdog

The Watchdog block inside CCONT contains a watchdog counter and some additional logic, which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low, - the WD–counter runs during that time, though. Watchdog counter is reset internally to 32 sec. at power up.

Digital Control

The MAD2WD1 ASIC, which consists of a MCU, a system ASIC and a DSP, controls the baseband functions.

MAD2WD1

MAD2WD1 contains following building blocks:

- ARM RISC processor with both 16-bit instruction set (THUMB mode) and 32-bit instruction set (ARM mode)
- TI Lead DSP core with peripherals
- BUSC (Bus Controller for controlling accesses from ARM to API, System Logic and MCU external memories, both 8- and 16-bit memories)
- System Logic

The MAD2WD1 operates from a 13 MHz system clock, which is generated by an internal 'divide by 2' circuit in the HAGAR RF-ASIC. Input to the HAGAR divider is from the 26Mhz VCXO frequency. The MAD2WD1 supplies a 13 MHz internal clock for the MCU and system logic blocks and a 13 MHz clock for the DSP, where it is multiplied to 45.5 MHz DSP clock (13MHz x 7/2).

The system clock is stopped in sleep-mode by disabling the VCXO supply from the CCONT regulator output (VR1). The CCONT provides a 32 kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.
MAD2WD1 supply voltages are VBB for I/O and VCORE for Internal functions as CPU, DSP and System Logic.

Memory

The MCU program code resides in an external flash program memory, which size is 16Mbits (1024k x 16bit). The MCU work (data) memory size is 1024 kbits (64k x 16bit).

The Bus Controller (BUSC) section in the MAD2WD1 decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip-select signals. BUSC supports a programmable number of wait states for each memory range.

Program and Data Memory

The MCU program code resides in the program memory which is a 32Mbits (2048k x 16bit) Flash memory.

Nonvolatile data memory is implemented with program (Flash) memory. Special EEPROM emulation (EEEMmu) software is utilized.

Work Memory

The work memory is a static RAM of size 2048k (128k x 16). The memory contents are

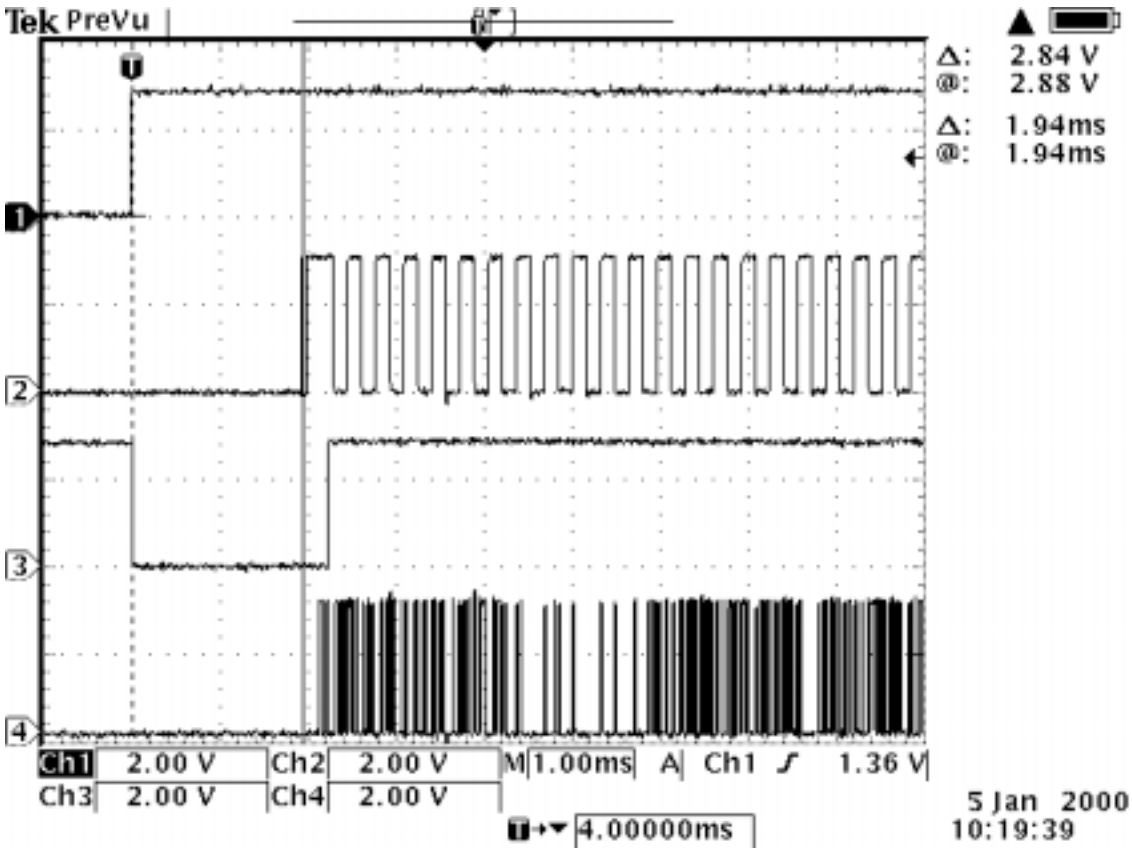
lost when the baseband voltage is switched off. All retainable data is stored in the data memory (Flash) when the phone is powered down.

MCU Memory Map

MAD2WD1 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 8-bit/16-bit databus.
The BUSC bus controller supports 8- and 16-bit access for byte, double byte, word and double word data.

Flash Programming

The Flash Program Voltage (VPP) is either internal (VBB= 2.8V)



Ch1: PURX (R307)	Ch3: F_Tx (X202, pin7)
Ch2: Mbus (X202, pin 3)	Ch4: F_Rx (X202, pin 8)

Figure 12: Flash Programming Sequence

COBBA GJP

COBBA GJP ASIC provides an interface between the baseband and the RF-circuitry. COBBA performs the analogue to digital conversion of the received signal.

Real time clock

The Real Time Clock (RTC) comprises a basic clock (hours and minutes), a calendar and a

timer with alarm and power on/off -function and miscellaneous calls. The RTC contains only the time base and the alarm timer but all other functions (e.g. calendar) are implemented with the MCU software.

The RTC is integrated in the CCONT, because the CCONT already contains the power up/down functions and a 32kHz sleep-clock, which is always running when the phone battery is connected. The 32 KHz sleep-clock is used as time source to a RTC block.

RF Module

This RF module executes all the RF functions of EGSM/DCS1800 dualband engine. RF circuitry is located on one side of the 8-layer transceiver-PWB. The RF design is based on the dualband direct conversion RF-IC "Hagar". There is no intermediate frequency.

EMC emissions are eliminated by metal shielding cans, which screen the transceiver. Internal screening is realized by separating different sections of the RF by shielding cans. The VCO is isolated from Hagar and external components by a can in the Hagar shielding can and PA, RX/TX Switch and LNA's are located in a separate can. The baseband circuitry is located on the same side of the same board, but in a separate shielding can.

Schematic diagrams in A3 size are included in this manual.

Maximum Ratings

Table 11: RF max ratings

Parameter	Rating
Battery voltage, idle mode	5.2 V (charging)
Regulated supply voltage	2.8 +/- 3% V
Voltage reference	1.5 +/- 1.5% V
Operating temperature range	-10...+55 deg. C
Absolute maximum battery voltage	4.2 V (charging)

RF Characteristics

Table 12: RF Characteristics

Item	Values (EGSM / DCS1800)
Receive frequency range	925... 960 MHz / 1805... 1880 MHz
Transmit frequency range	880... 915 MHz / 1710... 1785 MHz
Duplex spacing	45 MHz / 95 MHz
Channel spacing	200 kHz
Number of RF channels	174 / 374
Power class	4 (EGSM900) / 1 (DCS1800)
Number of power levels	15 / 16

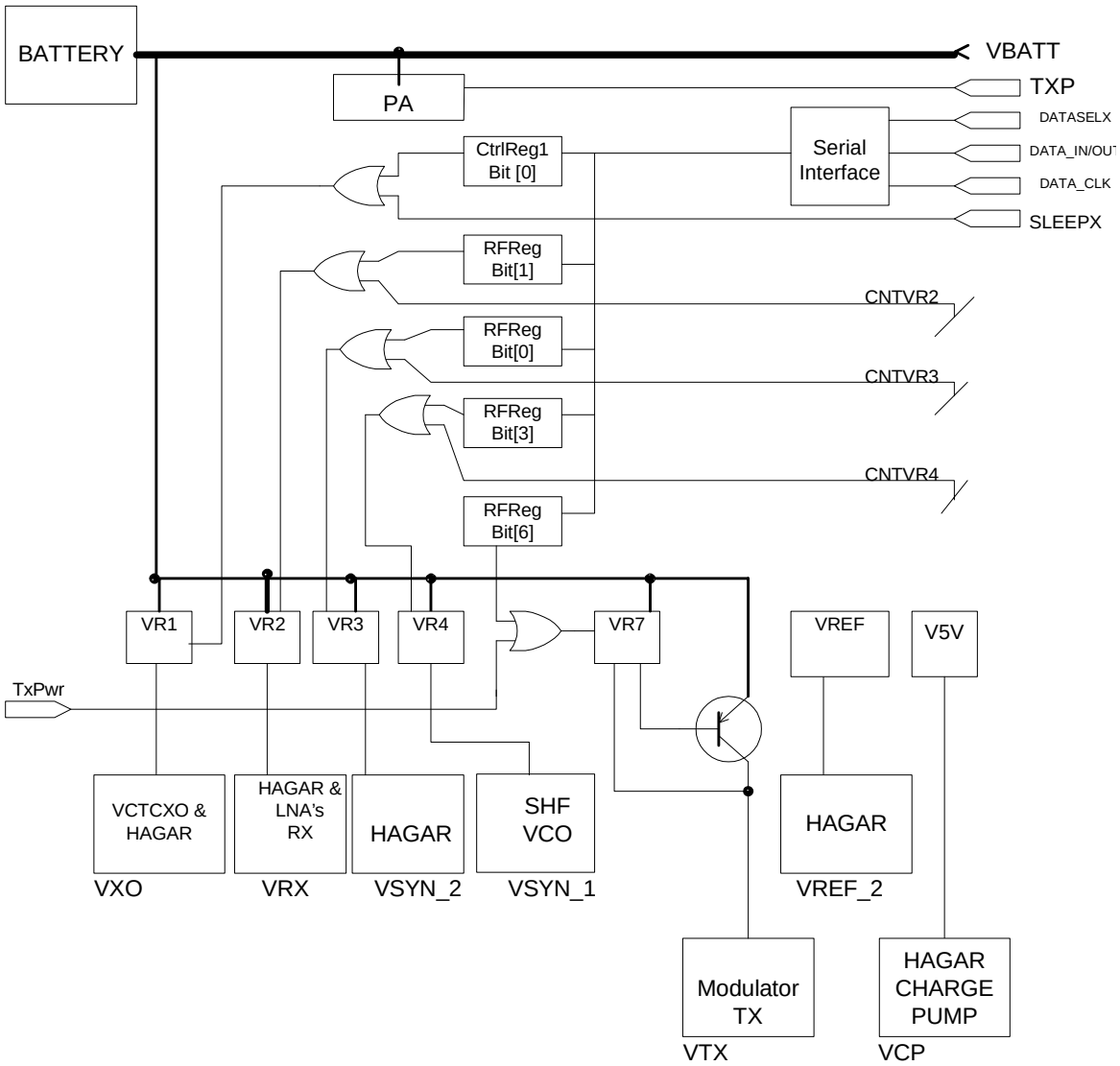
DC characteristics

Regulators

Transceiver has a multi function power management IC at baseband section, which contains among other functions, also 7 pieces of 2.8 V regulators.

VREF from CCONT IC and VREF RX from COBBA IC are used as the reference voltages for HAGAR RF-IC, VREF (1.5V) for bias reference and VREF RX (1.2V) for RX ADC's reference.

Figure 13: Power Distribution Diagram



Frequency Synthesizer

VCO frequency is locked with PLL into stable frequency source, which is a VCTCXO-module. VCTCXO is running at 26 MHz. Temperature effect is controlled by AFC voltage. VCTCXO is locked into frequency of the base station. AFC is generated by baseband with an 11 bit conventional DAC in COBBA.

PLL is located in HAGAR RF-IC and is controlled via serial bus from COBBA-IC (baseband).

Receiver

The receiver is a direct conversion, dualband linear receiver. Received RF-signal from the antenna is fed via RX/TX switch to 1st RX SAW filter and LNA's (low noise amplifier), sep-

arate branches for EGSM900 and DCS1800. Gain selection control of LNA's comes from HAGAR IC. Gain step is activated when RF-level at the antenna is about -45 dBm.

After the LNA the amplified signal (with low noise level) is fed to bandpass filter (2nd RX SAW filter). RX bandpass filters defines how good suppression of blocking signals outside receive band and the protection against spurious responses.

After the bandpass filters the signals are fed to baluns which converts the single ended signal to balanced. The balanced signal is fed to the RF input of Hagar. Differential RX signal is amplified and mixed directly down to BB frequency in HAGAR. Local signal is generated with external VCO. VCO signal is divided by 2 (DCS1800) or by 4 (EGSM900). PLL and dividers are in HAGAR-IC.

From the mixer output to ADC input RX signal is divided into I- and Q-signals. Accurate phasing is generated in LO dividers. After the mixer DTOS amplifiers convert the differential signals to single ended. DTOS has two gain stages. The first one has constant gain of 12dB and 85kHz cut off frequency. The gain of second stage is controlled with control signal g10. If g10 is high (1) the gain is 6dB and if g10 is low (0) the gain of the stage is -4dB.

The active channel filters in HAGAR provides selectivity for channels (-3dB @ +/-100 kHz typ.). The integrated base band filter is an active-RC-filter with two off-chip capacitors.

Integrated resistors and capacitors are tunable. These are controlled with a digital control word via Hagar serial interface. The correct control words that compensate for the process variations of integrated resistors and capacitors and of tolerance of off chip capacitors are found during RX filter calibration.

Next stage in the receiver chain is the AGC-amplifier, also integrated into HAGAR. The AGC has digital gain control via serial mode bus from COBBA IC.

Single ended filtered I/Q-signal is then fed to ADCs in COBBA-IC. Input level for ADC is 1.4 Vpp max.

Transmitter

Transmitter chain consists of final frequency IQ-modulator, dualband power amplifier and a power control loop.

I- and Q-signals are generated by baseband also in COBBA-ASIC. After post filtering (RC-network) they go into IQ-modulator in HAGAR. LO-signal for modulator is generated by VCO and is divided by 2 or by 4 depending on system mode, EGSM/DCS1800. After modulator the TX-signal is amplified and buffered. There are separate outputs for both EGSM and DCS1800. HAGAR TX output level is 5 dBm.

Next TX signals are converted to single ended by baluns. Then TX signals are amplified and buffered in discrete buffers. In EGSM branch there is a SAW filter after the balun.

The final amplification consists of a dualband power amplifier. It includes one 50 ohm input and two 50 ohm outputs. There is also a gain control, which is controlled with a power control loop in HAGAR. PA is able to produce over 2 W (3 dBm input level) in EGSM band and over 1 W (6 dBm input level) in DCS1800 band into 50 ohm output.

Power control circuit consists of discrete power detector (common for EGSM and DCS1800) and error amplifier in HAGAR. There is a directional coupler connected between PA output and RX/TX switch. It is a dualband type and has input and outputs for both systems. A coupler takes a sample from the forward going power with certain ratio. This signal is rectified in a schottky-diode and it produces a DC-signal after filtering.

This detected voltage is compared in the error-amplifier in HAGAR to TXC-voltage, which is generated by DA-converter in COBBA. Burst is enabled and set to rise with TXP until the output level is high enough for the feedback loop. Loop controls the output via the control pin in PA to the desired output level and burst has got the waveform of TXC-ramps.

Power control loop in HAGAR has two outputs, one for each frequency band.

AGC strategy

AGC-amplifier is used to maintain output level of the receiver in a certain range.

There is 50 dB accurate gain control (10 dB steps) and one larger step (~30 dB) in LNA.

AFC function

AFC is used to lock the transceiver frequency to the frequency of the base station. AFC-voltage is generated in the COBBA with 11 bit DA-converter. There is a RC-filter in AFC control line to reduce the noise from the converter. The AFC tracks the base station frequency continuously.

DC-compensation

DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging the large external capacitors in AGC stages to a voltage which cause a zero dc-offset. DCN2 set the signal offset to constant value (VREF RX 1.2 V).

Receiver Characteristics

Table 13: Receiver Characteristics

Item	Values
Type	Direct conversion, Linear, DualBand, FDMA/ TDMA
LO frequencies	3700... 3840 MHz / 3610... 3760 MHz
Typical 3 dB bandwidth	+/- 104 kHz
Sensitivity	min. - 102 / - 102 dBm (EGSM/PCN), S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	90 dB
Receiver output level (RF level -95 dBm)	350 mVpp, single ended I/Q-signals to RX ADCs
RSSI dynamic range	-110... -48 dBm
Compensated gain variation in receiving band	+/- 1.0 dB

Transmitter Characteristics

Table 14: Transmitter Characteristics

Item	Values
Type	Direct conversion, dualband, non-linear, FDMA/TDMA
LO frequency range	3520... 3660 / 3420... 3570 MHz
Output power	2 W / 1 W peak
Gain control range	min. 30 dB
Maximum phase error (RMS/peak)	max 5 deg./20 deg. Peak

User Interface features

MA4 module comprises the following user interface features:

- - Backlight circuit (for Keyboard and Display
- - Power key
- - UI switch

The remaining UI features are described in the manual section “User Interface Module MU4*.

Power key

The power key is connected between the GND and CCONT pin ‘PWRONX/WDDISX’. The power key is active in LOW state.

Backlight for display and keyboard

Display Backlight comprises 4 LEDs connected in parallel (in bottom of the Display).

Keyboard Backlight comprises 4 LEDs connected in parallel.

Color of all LEDs is yellow-green, l = 570nm

Switching circuits for Display and keyboard backlight is controlled by the same signal: KBLIGHTS.

KBLIGHT-signal = HIGH -> the lights are on

KBLIGHT-signal = LOW -> the lights are off.

UISWITCH is used for controlling backlight.

UI switch

The UISWITCH is an integrated switch IC for UI (user interface) purposes. It includes control switch for buzzer and vibra, LED-control (display & keyboard) and two current sinks for LED's.

Features:

- 2 adjustable constant current sink (60mA each) for keyboard and LCD-LEDs

- LED ON/OFF control (separated for keyboard and LCD)

- Buzzer ON/OFF control

- FET switch (low Rds-on) for buzzer current

- Vibra ON/OFF control

- FET switch for vibra current

- Thermal shutdown

- Power down function for optimum current consumption

- Package TSSOP20 because of 1.5mm height requirement

Audio and Vibrator

Vibrator and some of the audio parts are implemented on the same PCB board as BB-module and RF-module. The UI module comprises also Audio parts, including all stereo audio components. Kindly refer to the manual section "UIF module MU4"

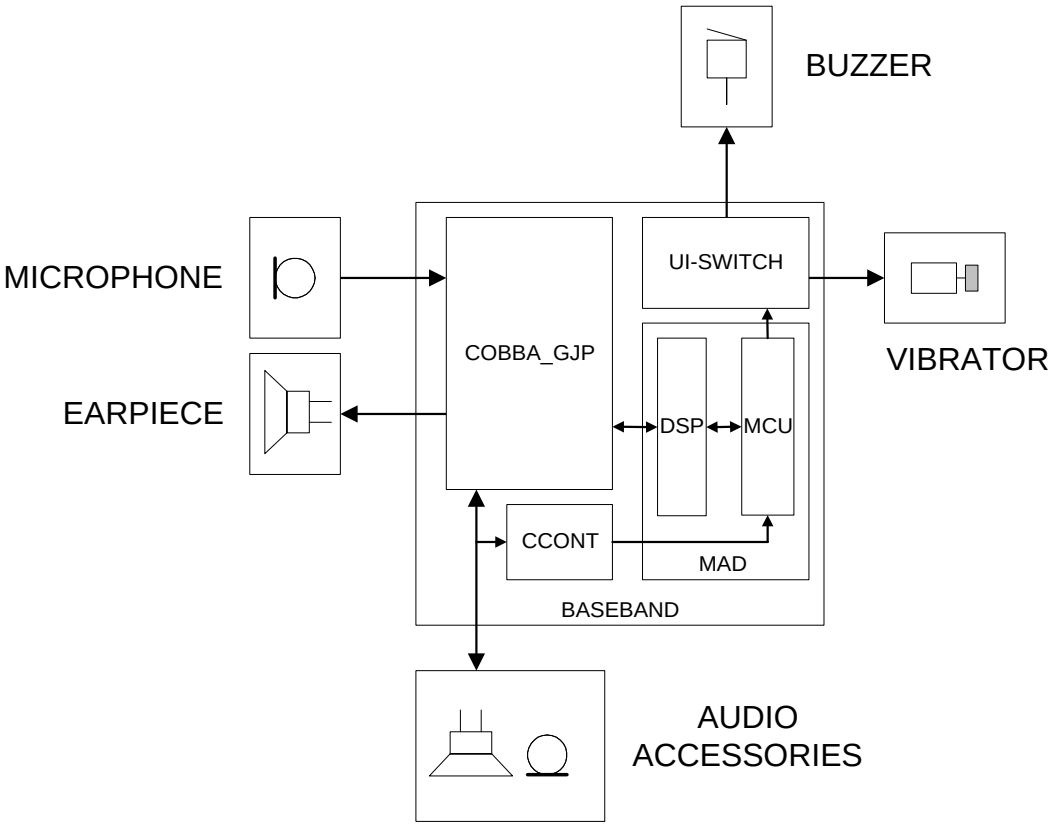


Figure 14: Audio / Vibrator Schematic

Audio Function Description

Audio control

The audio control and processing are taken care by the COBBA-GJP, which contains the audio (and RF) codec; and MAD2. MAD2 contains MCU and DSP blocks, handling and processing the audio signals.

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or a handsfree-unit (PPH-1) microphone. The microphone signals from different sources are connected to separate inputs at the COBBA-GJP ASIC. Inputs for the microphone signals are differential type.

MIC1 input is used for the microphone output of a handsfree unit. The internal microphone is connected to the MIC2 input, and the MIC3 is used for the headset.

In COBBA there are also three audio signal outputs of which the dual ended (and not differential!) EAR lines are used for internal earpiece and HF lines for accessory audio output. The third audio output, AUXOUT, is used for bias supply to the headset microphone.

Input and output selection and gain control is performed inside the COBBA-GJP ASIC according to control messages from the MAD2. DTMF and other audio tones are generated and encoded by the MAD2 and transmitted to the COBBA-GJP for decoding.

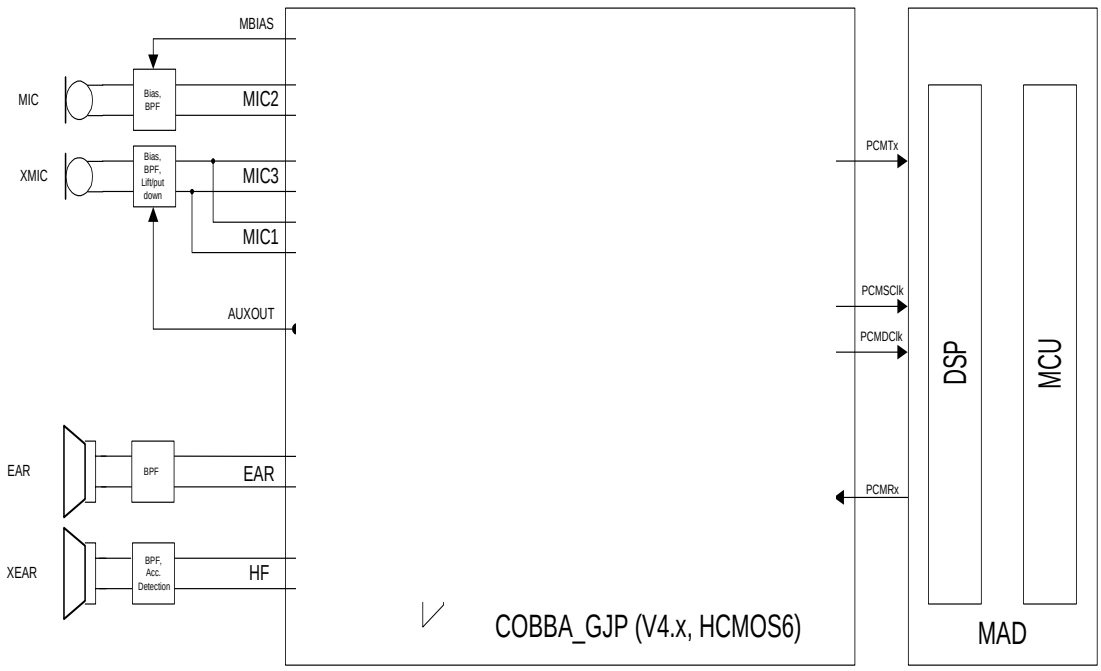


Figure 15: Audio Block Diagram (version 4)

Internal Audio Devices

Audio features of the CMT module are described in the following sections.

Ear Piece

The low impedance, dynamic type earphone is connected to the differential output (EAR) in the COBBA, the audio CODEC. The earpiece component resides on the UI module and the EAR+ and EAR- signals are routed to the UI module via the 36-pin board-to-board connector.

Earpiece Electric Interface

The low impedance, dynamic type earphone is connected to the differential output (EAR) in the COBBA, the audio CODEC.

Microphone

An omni directional microphone is used. The microphone is placed in the system connector sealed in its rubber gasket. The sound port is provided in the system connector.

Buzzer

Alerting tones and/or melodies are generated by a buzzer, which is controlled by a PWM signal from the MAD via an UI-SWITCH. The SPL requirement is 102dB (A) at 5cm. (Marketing target 105dB(A))

Buzzer is designed to be placed on the D-cover and fastened to it by two wings. The sound holes are placed in the A-cover.

The buzzer is lifted up from the PCB to find extra room on the PCB for the other BB components. The buzzer is electrically connected to the PCB by spring contacts.

Buzzer Electric Interface

The electric interface is shown below and the tables that follow show the relevant electrical specifications.

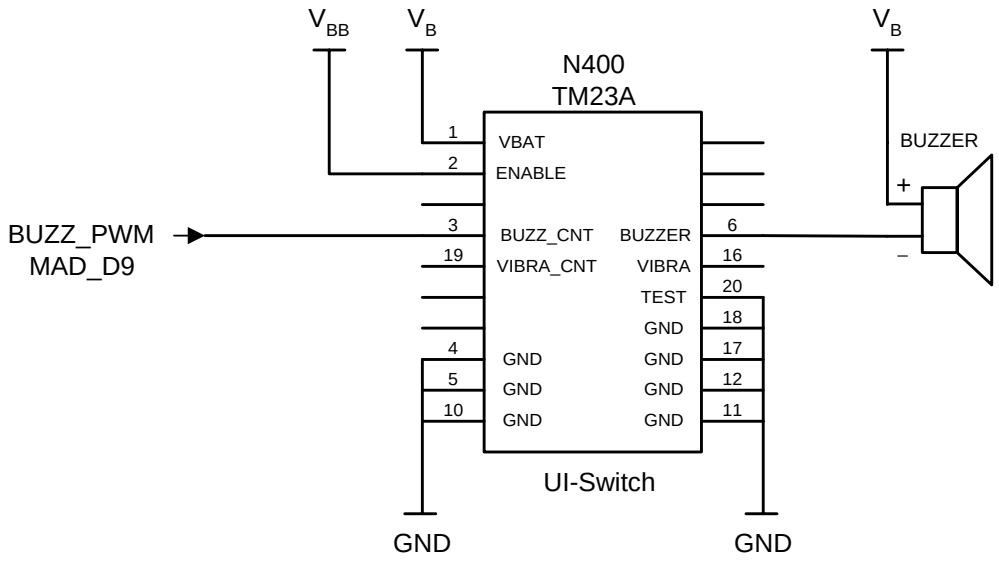


Figure 16: Buzzer Electrical Interface

Table 15: Interface-MAD and UI Switch

Signal	Parameter	Min.	Typ	Max	Unit
BUZZ_PWM Buzzer Control Signal From the MAD	PWM low level, logic low	0	0.2	0.5	V
	PWM high level, logic high	2.0	2.5	2.9	V
	Current MAD output			2	mA
	Buzzer PWM frequency	100		10000	Hz
	PWM duty cycle (256 linear steps)	0		100	%
BUZZ_CNT Buzzer Control Signal in the UI-Switch	PWM low level, logic low	0		0.5	V
	PWM high level, logic high	2.00	2.80	2.85	V
	Internal Pulldown Resistor	60	100	180	kΩ

Table 16: Interface -Ui Switch and buzzer

Signal	Parameter	Min.	Typ	Max	Unit	Notes
VBAT	Supply Voltage	3	3.6	5.2	V	
GND	Ground		0		V	
BUZZER	Buzzer Average Current			90	mA	50%dc@3.6v

Audio Accessories

The external audio interface supports the following accessories:

HDC-5: Headset with button

Headset is the most simple audio accessory to use. It merely only consists of an earpiece and a microphone, and a switch which in technical terms is often referred to as a HOOK-switch or HeadSet button. The HOOK-switch can be used either to answer in-coming calls or to end a call.

HDC-5 is purely a **passive audio accessory**.

HDD-2: **Stereo headset with button**

Functionally similar to HDC-5 but has twin plugs and earpieces.

LPS-3: **Loopset**

LPS-3, an accessory for hearing aid users, is detected and handled as the HDC-5. A current loopset, driven by a current amplifier, is used here instead of the earpiece.

External Mono Audio Interface

The interface is basically a 4-wire solution which gives two completely separate audio-paths, microphone- and earpiece-signals.

The interface is split up into:

External earpiece / speaker: **XEARP** (external earpiece, positive)

XEARN (external earpiece, negative)

External microphone: **XMICP** (external microphone, positive)

XMICN (external microphone, negative)

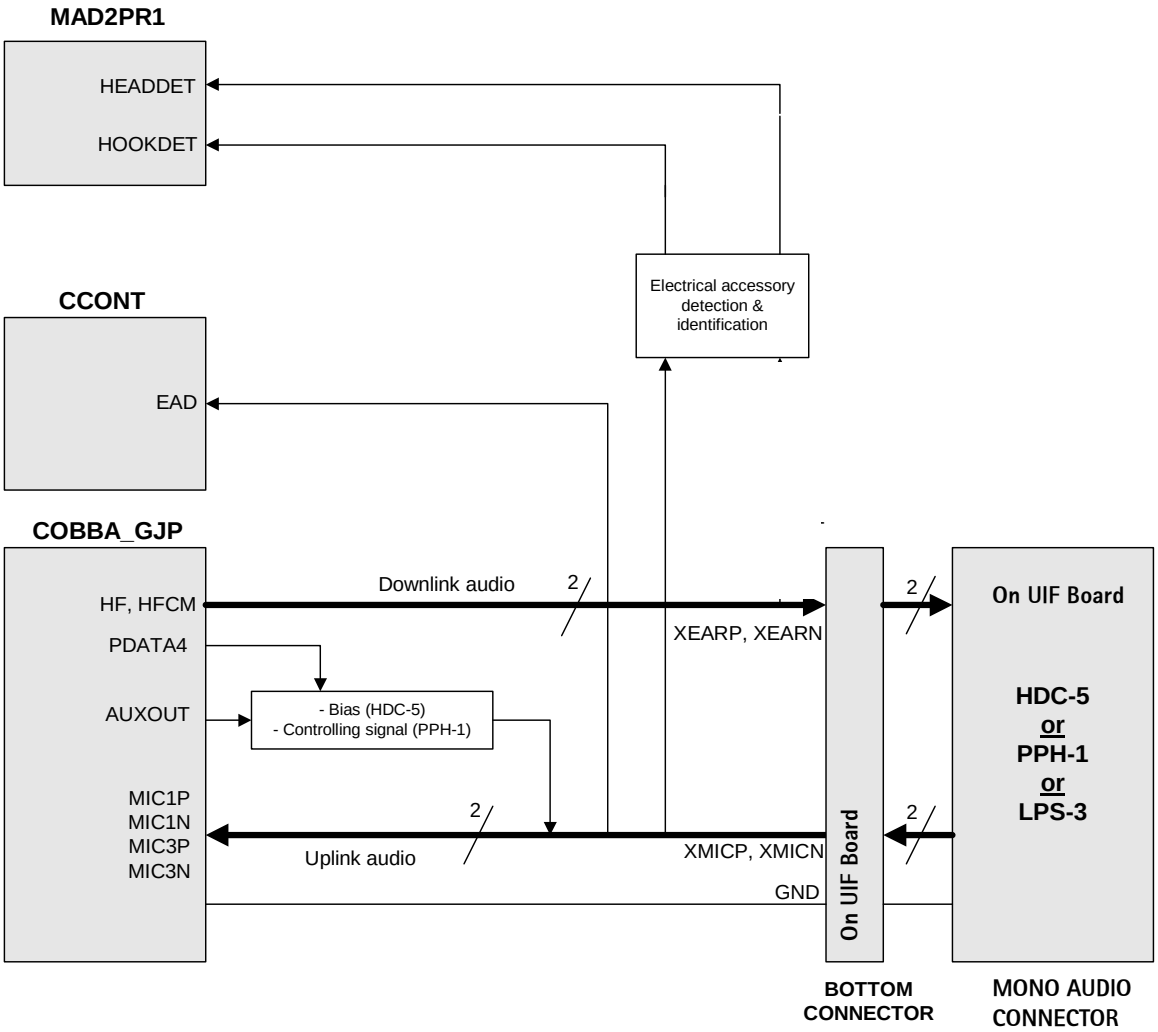


Figure 17: External Audio Interface- Block Diagram

The audio is analogue only.

External Mono Audio Interface — Electrical Interface

The external audio connections are presented in the following two diagrams. A headset or a handsfree can be connected directly to the system connector. The headset microphone bias is supplied from COBBA AUXOUT output and fed to the microphone through XMICP line.

HEADDET and **HOOKDET** are both the same type of 'interrupts input' in MAD.

If operating outside the ranges 0-0.8 V_{DC} or 1.8-2.8V_{DC} the interrupt inputs will start pulling current.

EAD is an analogue input on CCONT used to measure the DC-voltage on MIC1P line. This voltage value is used to identify the accessories and to control their function.

HF and **HFCM** are two audio outputs through which audio can be routed to either HS-earpiece or PPH-1 speaker. HF and HFCM are externally wired as fully- differential outputs, however it is only HF which in reality performs the audio-amplification.

MIC1P, MIC1N, MIC3P and **MIC3N** are all inputs to the microphone amplifier in COBBA. In short form the main difference for the listed inputs are:

- MIC1P, MIC1N: Rated to audio signals up to 2 Vpp. Used for PPH-1 microphone.
- MIC3P, MIC3N: Rated to audio signals up to 200 mVpp. Used for HS microphone.

AUXOUT is an output having two functions in the Accessory interface:

Controlling purposes for the PPH-1. AUXOUT can be set to the following states by the MCU-SW:

- High Impedance (Z)
- 2.1 Vdc
- 1.5 Vdc
- Low Impedance (0 Vdc)

External Mono Audio Connector (on the UI module)

The accessibility to the external audio interface is reached by the system connector, containing a 4-pole Jack plug. The Jack plug which is integrated in the system connector contains a mechanical switch which is used to detect the connection of the accessories.

The configuration for the 4-pole Jack-plug is shown in the following figure.

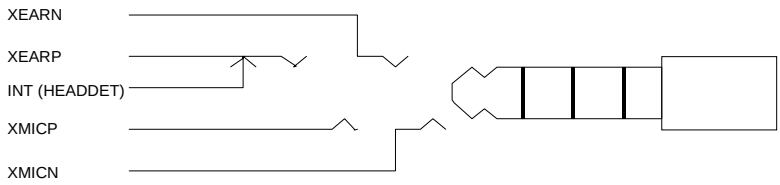


Figure 18: 4 Pole Jack plug for audio accessories

External Audio Signal Electrical Specifications

Table 17: External Audio Signals - Electrical Specifications

Name	Min.	Typ	Max	Unit	Notes
XMICP & XMICN		2.2		kΩ	Input AC impedance
			1	Vpp	Maximum signal level
		2.1		V	Output DC level
			500	µA	Bias current
XEARP & XEARN		47		W	Output AC impedance (ref. GND)
		10		µF	Series output capacitance (ref. GND)
		2.8		V	DC voltage (330k pull-up to VBB) (When accessory is not connected!)
HEADDET			9.15	uA	When accessory is not connected.
VIN	0		12	V	Charger Input Voltage
GND	0		0.3	V	Ground

Accessory Detection, Identification and Control

Accessory Detection

XEARP signal has a 300k pull-up (R203) and 100k pulldown resistor (R109). By these the HEADDET is pulled up when **an accessory is connected**, and pulled down when **disconnected**. See Figure 29, "External Audio Interface - Speaker," on page 59. (The system connector must be assembled otherwise the transceiver will assume that some accessory is connected!)

Table 18: HOOKDET and HEADDET Truth Table

Accessory connected	HeadDet	Notes
No accessory connected	Low	-
An accessory connected	High	XEAR and XMIC loaded (dc)

Accessory Identification

The voltage level on XMICP signal is measured by CCONT at its ADC input, EAD. This voltage level is used to determine the **type of accessory**. For details see DOC. DHJ00143-EN, HD947/Basic implementation of Janette accessory interface.

Accessory Control

Headset

In the HDC-5 the HeadSet-button is electrically connected across the XMICP and XMICN lines). When the HeadSet button is activated, a change in the current through the microphone's bias resistors appears. Based on this change, a transistor-switch (V100) controls the logic state of the HOOKDET in the MAD (See Figure 28, "External Audio Interface - Microphone," on page 59). When the switch on the headset is pressed, the switch (V100) goes on and the HOOKDET will go to the low level state. This is used **to lift the receiver or to put it down.**

(The voltage value at EAD input is used to control if the Headset remains connected. The voltage at EAD can also be used to detect a keypress, but it can fails, if the key is pressed with a low interval

Table 19: Detection of Handset keypress

	HS button	HOOKDET	EAD
AUXOUT = 'Z' (HS Connected)	Open	H	-
	Closed	H	-
AUXOUT = 2.1Vdc (HS Connected)	Open	H	≈ 750 - 1050 mVdc
	Closed	L	≈ 600 - 700 mVdc

Accessories Electric Specifications

Table 20: HDC-5 Electrical Specifications

	Min.	Typ	Max	Comment
Impedance, Transmitting	1540 ΩΩ	2200 ΩΩ	2860 ΩΩ	
MIC Bias		2.1 V		
HDC-5 microphone current			400 μμA	
Impedance, Receiving	112 ΩΩ	150 ΩΩ	188 ΩΩ	
HDC-5 button closed resistor		2 × 22 ΩΩ		±± 5%

Vibra Alerting Device

A vibra alerting device is used to generate a vibration signal for an incoming call. Vibra is located in the phone. The vibra is controlled by a PWM signal from the MAD and via the UI-SWITCH.

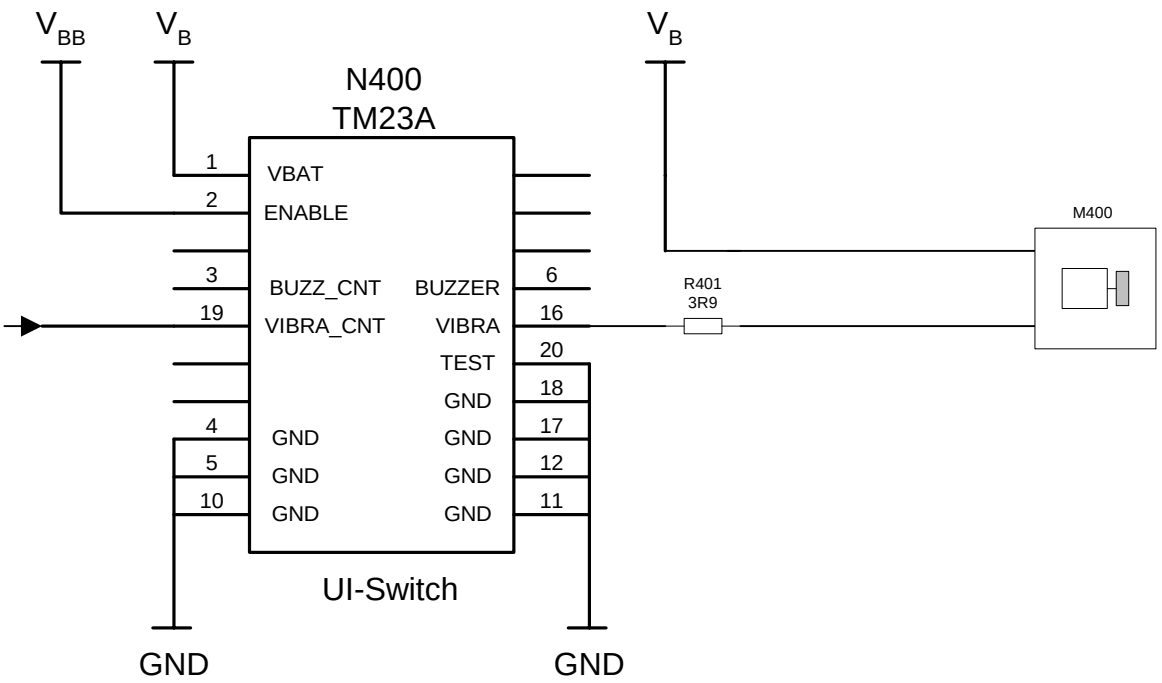


Figure 19: Vibrator Electrical Interface

Table 21: Interface -MAD UI Switch

Signal	Parameter	Min.	Typ	Max	Unit	Notes
VIBRA_PWM Vibra Control Signal From MAD	PWM low level, logic low	0	0.2	0.5	V	
	PWM high level, logic high	2.0	2.5	2.9	V	
	Current MAD output			2	mA	
	Vibra PWM frequency		22k		Hz	
VIBRA_CNT Vibra Control Signal in UI-Switch	PWM low level, logic low	0		0.5	V	
	PWM high level, logic high	2.00	2.80	2.85	V	
	Internal Pulldown Resistor	60	100	180	kΩ	

Table 22: Interface - UI Switch and Vibra

Signal	Parameter	Min.	Typ	Max	Unit	Notes
VBAT	Supply Voltage	3	3.6	5.2	V	
GND	Ground		0		V	
VIBRA	Vibra Nominal Current		120		mA	3.6V@10Ω
	Vibra Start Current			175	mA	5.2V
	Vibra Peak Current			190	mA	5.2V
	Vibra Reverse Peak Current			340	mA	
	Vibra FET Switch R_{dson}			1	W	

Parts Lists

CMT module MA4 (0201794)

EDMS issue 4.1

Item	Code	Standard description	Value, Note
A101	9517062	pa shield assy	DMC02526-
A102	9517064	Rf shield assy	DMC02527-
A103	9517063	bb shield assy	DMC02525-
B200	4510293	Crystal	32.768KHZ+-20PPM
C100	2315211	Chip array x5r 2x100n y	Y
C102	2315203	Chip array x5r 2x10n m 1	1
C103	2315201	Chip array np0 2x27p k 2	2
C109	2315209	Chip array x5r 2x33n m 1	1
C110	2315259	Chip array x5r 2x33n k 1	1
C111	2320744	Chipcap x7r 1n0 k 50v	
C113	2320481	Chipcap x5r 1u k 6v3	
C114	2320546	Chipcap np0 27p j 50v	
C115	2320546	Chipcap np0 27p j 50v	
C116	2320805	Chipcap x5r 100n k 10v	
C117	2320805	Chipcap x5r 100n k 10v	
C119	2320805	Chipcap x5r 100n k 10v	
C120	2315259	Chip array x5r 2x33n k 1	1
C121	2320778	Chipcap x7r 10n k 16v	
C124	2315201	Chip array np0 2x27p k 2	2
C126	2320744	Chipcap x7r 1n0 k 50v	
C128	2610031	Chiptcap 10u m 10v 2r	(
C200	2312211	Chipcap x5r 3u3 k 6v3	
C201	2312211	Chipcap x5r 3u3 k 6v3	
C202	2320540	Chipcap np0 15p j 50v	
C203	2320602	Chipcap np0 4p7 c 50v	
C204	2320805	Chipcap x5r 100n k 10v	
C207	2320481	Chipcap x5r 1u k 6v3	
C208	2320744	Chipcap x7r 1n0 k 50v	
C209	2320481	Chipcap x5r 1u k 6v3	
C210	2320805	Chipcap x5r 100n k 10v	
C211	2320744	Chipcap x7r 1n0 k 50v	
C212	2320805	Chipcap x5r 100n k 10v	
C213	2320481	Chipcap x5r 1u k 6v3	
C214	2320744	Chipcap x7r 1n0 k 50v	
C215	2312413	Chipcap x7r 220n m 50v	
C216	2320546	Chipcap np0 27p j 50v	

Item	Code	Standard description	Value, Note
C217	2320546	Chipcap np0 27p j 50v	
C218	2310793	Chipcap x5r 2u2 k 10v	
C219	2610031	Chiptcap 10u m 10v 2r	(
C220	2320508	Chipcap np0 1p0 c 50v	
C221	2320560	Chipcap np0 100p j 50v	
C223	2320546	Chipcap np0 27p j 50v	
C224	2320805	Chipcap x5r 100n k 10v	
C225	2312401	Chipcap x5r 1u0 k 10v	
C226	2320805	Chipcap x5r 100n k 10v	
C227	2312211	Chipcap x5r 3u3 k 6v3	
C228	2312211	Chipcap x5r 3u3 k 6v3	
C229	2320548	Chipcap np0 33p j 50v	
C230	2320538	Chipcap np0 12p j 50v	
C231	2320560	Chipcap np0 100p j 50v	
C232	2315201	Chip array np0 2x27p k 2	2
C233	2312211	Chipcap x5r 3u3 k 6v3	
C234	2320805	Chipcap x5r 100n k 10v	
C235	2315201	Chip array np0 2x27p k 2	2
C236	2315203	Chip array x5r 2x10n m 1	1
C239	2320481	Chipcap x5r 1u k 6v3	
C240	2320481	Chipcap x5r 1u k 6v3	
C241	2320481	Chipcap x5r 1u k 6v3	
C242	2320481	Chipcap x5r 1u k 6v3	
C243	2320481	Chipcap x5r 1u k 6v3	
C246	2320481	Chipcap x5r 1u k 6v3	
C247	2611753	Chiptcap 33u m 16/8v 6.	6.
C303	2320552	Chipcap np0 47p j 50v	
C304	2320546	Chipcap np0 27p j 50v	
C305	2320546	Chipcap np0 27p j 50v	
C306	2315211	Chip array x5r 2x100n y	Y
C307	2320805	Chipcap x5r 100n k 10v	
C308	2320805	Chipcap x5r 100n k 10v	
C311	2320805	Chipcap x5r 100n k 10v	
C313	2320805	Chipcap x5r 100n k 10v	
C315	2320805	Chipcap x5r 100n k 10v	
C316	2320805	Chipcap x5r 100n k 10v	
C317	2320778	Chipcap x7r 10n k 16v	
C318	2320805	Chipcap x5r 100n k 10v	
C400	2320604	Chipcap np0 18p j 50v	
C404	2312401	Chipcap x5r 1u0 k 10v	
C407	2320744	Chipcap x7r 1n0 k 50v	
C408	2315205	Chip array x5r 2x1n m	16
C500	2312211	Chipcap x5r 3u3 k 6v3	
C501	2312211	Chipcap x5r 3u3 k 6v3	

Item	Code	Standard description	Value, Note
C502	2320778	Chipcap x7r 10n k 16v	
C503	2320554	Chipcap np0 56p j 50v	
C504	2320620	Chipcap x7r 10n j 16v	
C505	2320546	Chipcap np0 27p j 50v	
C506	2320620	Chipcap x7r 10n j 16v	
C507	2320520	Chipcap np0 2p2 c 50v	
C508	2315109	Chip array x5r 4x100n k	K
C509	2320540	Chipcap np0 15p j 50v	
C510	2320560	Chipcap np0 100p j 50v	
C511	2320584	Chipcap x7r 1n0 j 50v	
C512	2315017	Chip array np0 4x470p j	J
C513	2320584	Chipcap x7r 1n0 j 50v	
C514	2315267	Chip array x5r 2x47n y 1	1
C515	2320520	Chipcap np0 2p2 c 50v	
C516	2320785	Chipcap x7r 47n k 10v	
C517	2320540	Chipcap np0 15p j 50v	
C518	2312211	Chipcap x5r 3u3 k 6v3	
C519	2320909	Chipcap np0 hq 1p0 b	16V
C520	2320534	Chipcap np0 8p2 c 50v	
C521	2320540	Chipcap np0 15p j 50v	
C522	2312211	Chipcap x5r 3u3 k 6v3	
C524	2320620	Chipcap x7r 10n j 16v	
C526	2315251	Chip array x5r 2x180p k	K
C527	2320536	Chipcap np0 10p j 50v	
C528	2320534	Chipcap np0 8p2 c 50v	
C529	2320783	Chipcap x7r 33n k 10v	
C530	2320778	Chipcap x7r 10n k 16v	
C531	2320524	Chipcap np0 3p3 c 50v	
C533	2320538	Chipcap np0 12p j 50v	
C534	2320602	Chipcap np0 4p7 c 50v	
C535	2320783	Chipcap x7r 33n k 10v	
C536	2320546	Chipcap np0 27p j 50v	
C537	2320540	Chipcap np0 15p j 50v	
C538	2320560	Chipcap np0 100p j 50v	
C539	2320778	Chipcap x7r 10n k 16v	
C540	2320540	Chipcap np0 15p j 50v	
C541	2320548	Chipcap np0 33p j 50v	
C542	2320560	Chipcap np0 100p j 50v	
C543	2312211	Chipcap x5r 3u3 k 6v3	
C544	2320778	Chipcap x7r 10n k 16v	
C545	2320602	Chipcap np0 4p7 c 50v	
C546	2320534	Chipcap np0 8p2 c 50v	
C547	2320540	Chipcap np0 15p j 50v	
C548	2320620	Chipcap x7r 10n j 16v	

Item	Code	Standard description	Value, Note
C549	2320584	Chipcap x7r 1n0 j 50v	
C550	2320524	Chipcap np0 3p3 c 50v	
C552	2320620	Chipcap x7r 10n j 16v	
C553	2320570	Chipcap x7r 270p j 50v	
C554	2320540	Chipcap np0 15p j 50v	
C555	2320544	Chipcap np0 22p j 50v	
C556	2320546	Chipcap np0 27p j 50v	
C557	2320580	Chipcap x7r 680p j 50v	
C558	2312217	Chipcap np0 10n j 16v	
C559	2320552	Chipcap np0 47p j 50v	
C560	2320552	Chipcap np0 47p j 50v	
C561	2320787	Chipcap x7r 15n k 16v	
C562	2312401	Chipcap x5r 1u0 k 10v	
C563	2320602	Chipcap np0 4p7 c 50v	
C564	2320584	Chipcap x7r 1n0 j 50v	
C565	2320787	Chipcap x7r 15n k 16v	
C566	2320540	Chipcap np0 15p j 50v	
C568	2320508	Chipcap np0 1p0 c 50v	
C569	2320556	Chipcap np0 68p j 50v	
C570	2320540	Chipcap np0 15p j 50v	
C571	2310793	Chipcap x5r 2u2 k 10v	
C572	2320548	Chipcap np0 33p j 50v	
C573	2320756	Chipcap x7r 3n3 k 50v	
C574	2320546	Chipcap np0 27p j 50v	
C575	2611755	Chiptcap 68u m 16v 6.	6.
C576	2320540	Chipcap np0 15p j 50v	
C577	2320508	Chipcap np0 1p0 c 50v	
C578	2320552	Chipcap np0 47p j 50v	
C579	2320546	Chipcap np0 27p j 50v	
C581	2320546	Chipcap np0 27p j 50v	
C582	2320552	Chipcap np0 47p j 50v	
C585	2320524	Chipcap np0 3p3 c 50v	
C586	2320548	Chipcap np0 33p j 50v	
C587	2320536	Chipcap np0 10p j 50v	
C588	2320536	Chipcap np0 10p j 50v	
C589	2320536	Chipcap np0 10p j 50v	
C590	2320604	Chipcap np0 18p j 50v	
C591	2320546	Chipcap np0 27p j 50v	
C592	2320604	Chipcap np0 18p j 50v	
C593	2320544	Chipcap np0 22p j 50v	
C597	2320602	Chipcap np0 4p7 c 50v	
C600	2320546	Chipcap np0 27p j 50v	
C601	2320546	Chipcap np0 27p j 50v	
C602	2320546	Chipcap np0 27p j 50v	

Item	Code	Standard description	Value, Note
C603	2320546	Chipcap np0 27p j 50v	
C604	2320546	Chipcap np0 27p j 50v	
C605	2320522	Chipcap np0 2p7 c 50v	
C606	2320524	Chipcap np0 3p3 c 50v	
D300	4370687	IC mad2wd1 v16 rom6	F741541
D301	4340997	Flash 2mx16 70ns 2.7v	B3
D302	4340899 4341615	IC p8/2001 pls SRAM 128X16 70ns 2.7-3-3v	Early versions TBGA48
D304	4340973	IC ncp305sq mcu reset	3.0V
F200	5119019	Sm fuse f 1.5a 32v 0603	0603
G500	4350249	VCO 3420-3840mhz 2.7v 20	20
G502	4510275	VCTXCO 26mhz+-5ppm 2.7v	2.7V
L200	3203725	Ferrite bead	600R/100MHZ
L201	3203705	Ferrite bead 0.015r /	42R/
L202	3203705	Ferrite bead 0.015r	42R/
L203	3646039	Chip coil 5n6 +-0n3	Q7/1
L500	3646091	Chip coil 6n8 j	Q27/800M
L502	3645249	Chip coil 3n9 j	Q22/250M
L504	3646067	Chip coil 18n j	Q29/800M
L506	3646061	Chip coil 15n j	Q30/800M
L507	3646091	Chip coil 6n8 j	Q27/800M
L508	3646039	Chip coil 5n6 +-0n3	Q7/1
L509	3646027	Chip coil 33n j	Q7/100MH
L510	3646007	Chip coil 27n j	Q27/800M
L511	3645073	Chip coil 10u k 0.015a 1	1
L512	3645117	Chip coil 5n6 +-0n3	Q8/1
L513	3203705	Ferrite bead 0.015r	42R/
L514	3645213	Chip coil 22n j	Q38/250M
L515	4551021	Dir.coupl.897.5/1747.5mh	
L516	3646055	Chip coil 8n2 j	Q28/800M
L520	3646065	Chip coil 12n j	Q31/800M
L600	3646009	Chip coil 10n j	Q30/800M
N100	4370643 4370793	Cobba_gjp v4.1 V257BG64T Cobba_gjp v4.1	Early versions V257JG64T/8
N200	4370621 4370807	Chaps v2.0 u423v20g36t CHAPS V3.1 TU01BALT	Early versions BGA36
N201	4370719	Ccont 2m	wfd163mg64t/8 L
N400	4370433	IC uiswitch	sttm23av20t
N500	4370781	IC hagar 5	tzc6begt
N502	4350259	IC pw amp 900/1800mhz 3	4DB34DBM
N503	4340797	IC lp2980im5x-4.7 reg	4.7V
R100	1620023	Res network 0w06 2x47k j	J
R101	1430816	Chipres 0w06 330k j	
R102	1430798	Chipres 0w06 56k j	

Item	Code	Standard description	Value, Note
R103	1620025	Res network 0w06	2x100k
R104	1430754	Chipres 0w06 1k0 j	
R105	1620105	Res network 0w06 2x2k2 j	J
R106	1620031	Res network 0w06 2x1k0 j	J
R107	1430804	Chipres 0w06 100k j	
R108	1430804	Chipres 0w06 100k j	
R109	1430804	Chipres 0w06 100k j	
R110	1620025	Res network 0w06 2x100k	2x100k
R111	1430788	Chipres 0w06 22k j	
R112	1430734	Chipres 0w06 220r j	
R114	1430778	Chipres 0w06 10k j	
R115	1620031	Res network 0w06 2x1k0 j	J
R119	1430710	Chipres 0w06 22r j	
R120	1430710	Chipres 0w06 22r j	
R200	1430728	Chipres 0w06 120r j	
R202	1430700	Chipres 0w06 10r j	
R203	1430816	Chipres 0w06 330k j	
R204	1419003	Chipres 0w5 0r22 j 200pp	200PP
R207	1430726	Chipres 0w06 100r j	
R208	1430764	Chipres 0w06 3k3 j	
R209	1430796	Chipres 0w06 47k j	
R210	1430770	Chipres 0w06 4k7 j	
R211	1430796	Chipres 0w06 47k j	
R212	1430826	Chipres 0w06 680k j	
R213	1430726	Chipres 0w06 100r j	
R214	1430325	Chipres 0w06 2m2 j	
R217	1620017	Res network 0w06 2x100r	2x100r
R218	1430871	Chipres 0w06 82k f	
R219	1430873	Chipres 0w06 27k f	
R220	1620019	Res network 0w06 2x10k j	J
R221	1430808	Chipres 0w06 150k j	
R222	1430804	Chipres 0w06 100k j	
R224	1430778	Chipres 0w06 10k j	
R301	1620017	Res network 0w06 2x100r	2x100r
R302	1430812	Chipres 0w06 220k j	
R303	1430788	Chipres 0w06 22k j	
R304	1620023	Res network 0w06 2x47k j	J
R307	1430770	Chipres 0w06 4k7 j	
R308	1430778	Chipres 0w06 10k j	
R309	1430754	Chipres 0w06 1k0 j	
R310	1430764	Chipres 0w06 3k3 j	
R312	1430754	Chipres 0w06 1k0 j	
R401	1411275	Chipres 0w25 3r9 j	
R402	1430726	Chipres 0w06 100r j	

Item	Code	Standard description	Value, Note
R403	1430778	Chipres 0w06 10k j	
R404	1430778	Chipres 0w06 10k j	
R406	1825033	Chip varistor vwm14v vc4	VC4
R407	1825033	Chip varistor vwm14v vc4	VC4
R414	1620031	Res network 0w06 2x1k0 j	J
R500	1620003	Res network 0w03 4x100r	4x100r
R504	1620019	Res network 0w06 2x10k j	J
R506	1430764	Chipres 0w06 3k3 j	
R507	1430778	Chipres 0w06 10k j	
R508	1430700	Chipres 0w06 10r j	
R509	1430803	Chipres 0w06 4k7 f 200pp	200PP
R510	1430762	Chipres 0w06 2k2 j	
R511	1430846	Chipres 0w06 2k7 f	
R512	1430187	Chipres 0w06 47k f 200pp	200PP
R513	1430700	Chipres 0w06 10r j	
R514	1430762	Chipres 0w06 2k2 j	
R515	1430770	Chipres 0w06 4k7 j	
R516	1430778	Chipres 0w06 10k j	
R517	1430778	Chipres 0w06 10k j	
R518	1430780	Chipres 0w06 12k j	
R519	1430718	Chipres 0w06 47r j	
R521	1430764	Chipres 0w06 3k3 j	
R522	1430788	Chipres 0w06 22k j	
R523	1430730	Chipres 0w06 150r j	
R524	1430730	Chipres 0w06 150r j	
R525	1430764	Chipres 0w06 3k3 j	
R526	1430708	Chipres 0w06 18r j	
R527	1430738	Chipres 0w06 270r j	
R528	1430738	Chipres 0w06 270r j	
R529	1430762	Chipres 0w06 2k2 j	
R530	1430734	Chipres 0w06 220r j	
R531	1430726	Chipres 0w06 100r j	
R532	1430726	Chipres 0w06 100r j	
R533	1430700	Chipres 0w06 10r j	
R534	1430754	Chipres 0w06 1k0 j	
R535	1430812	Chipres 0w06 220k j	
R536	1430734	Chipres 0w06 220r j	
R537	1430754	Chipres 0w06 1k0 j	
R538	1430762	Chipres 0w06 2k2 j	
R539	1430738	Chipres 0w06 270r j	
R540	1430734	Chipres 0w06 220r j	
R541	1620033	Res network 0w06 2x5k6 j	J
R542	1430710	Chipres 0w06 22r j	
R543	1430738	Chipres 0w06 270r j	

Item	Code	Standard description	Value, Note
R544	1430714	Chipres 0w06 33r j	
R545	1430730	Chipres 0w06 150r j	
R546	1430726	Chipres 0w06 100r j	
R547	1430718	Chipres 0w06 47r j	
R548	1620033	Res network 0w06 2x5k6 j	J
R550	1430700	Chipres 0w06 10r j	
R551	1430744	Chipres 0w06 470r j	
R552	1430744	Chipres 0w06 470r j	
R553	1430700	Chipres 0w06 10r j	
R554	1430726	Chipres 0w06 100r j	
R556	1430726	Chipres 0w06 100r j	
R557	1430832	Chipres 0w06 2k7 j	
R558	1430732	Chipres 0w06 180r j	
R559	1430754	Chipres 0w06 1k0 j	
R564	1430710	Chipres 0w06 22r j	
R601	1430716	Chipres 0w06 39r j	
R603	1430770	Chipres 0w06 4k7 j	
R604	1430786	Chipres 0w06 18k j	
R605	1430778	Chipres 0w06 10k j	
R606	1430718	Chipres 0w06 47r j	
S419	5209001	Sm sw tact spst 12v	50MA
T500	4550139	Transf balun	1.8GHZ+/-10
T501	4550129	Transf balun	900MHZ+/-10
T502	3640423	Transf balun	3.7GHZ+/-30
T503	4550139	Transf balun	1.8GHZ+/-10
T504	4550129	Transf balun	900MHZ+/-10
V100	4210100	Tr bc848w n 30v	0.1A100M
V101	4210121	Tr pmst6429 n45v hfe	<12
V102	4210049	Tr pdtc114ee n50v	RB=RBE
V103	4110601	Di fast 1ss355	80V0.1A<4
V200	4210401	Tr 2pa1774 p 50v0.15a	14
V201	1825005	Chip varistor vwm14v	VC3
V202	4110441	Sch di stps0520z 20v	0.5
V203	4113669	Zdix4 tvs/esd rsa6.1en	6
V204	4113669	Zdix4 tvs/esd rsa6.1en	6
V205	4219929	Trx2+4x10k n umh11	50V.0
V413	4113669	Zdix4 tvs/esd rsa6.1en	6
V414	4110601	Di fast 1ss355	80V0.1A<4
V500	4210261	Tr bga428 lna1.8ghz	19.5
V501	4210281	Tr bga2003 lna adj.	900M
V502	4210100	Tr bc848w n 30v 0.1a100m	0.1A100M
V503	4115881	Schdix2 nsr15dw1 <2pf	S
V601	4210197	Tr ne68119 n 7ghz lna	NF
V602	4210401	Tr 2pa1774 p 50v0.15a	14

Item	Code	Standard description	Value, Note
Z500	4511193	Dual rxsaw filter	900/1800
Z501	4511193	Dual rxsaw filter	900/1800
Z502	4550201	Dipl+2xsw880-960/1710-18	
Z503	4511183	Saw filter	897.5+-17.5MHZ/
	9854575	pwb ma4_04 108x41.6x1.0	108x41.6x1.0

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